Cross connection system for time-division multiplexed signal

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Provided is a cross connection system for time-division multiplexed signals, upon detection of deterioration in quality, performs line setting to easily switch to a line having another directional orientation. The cross connection system receives an SDH interface signal, separates a virtual container line signal that is multiplexed into the SDH interface signal and connects the virtual container line to one of a number of output terminals, and is constituted by a signal receiver for receiving a primary signal, for detecting alarm information contained in the primary signal that is received, and for performing conversion of the primary signal in consonance with an occasion when the alarm information is detected, a signal synchronizer for, upon receipt of the primary signal and the alarm signal from the signal receiver, switching phases for the primary signal and the alarm information by using a first clock and for outputting the results, and a TSI function section for exchanging the primary signals received from the signal synchronizer for individual time slots of the primary signals.

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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a cross connection (line setting) system for time-division multiplexed signals, and in particular to a cross connection system that includes a path switch in the exchange system for exchanging time-division multiplexed signals provided for an SDH (Synchronous Digital Hierarchy) network.

2. Related Arts

The SDH technique is an internationally standardized multiplex method that can be efficiently applied for telephone services and other services in transmission text data and picture image data.

In consonance with the progress that has been made in techniques concerning cross connection (line setting) apparatuses, a system where transmission lines for an entire network can be freely changed and improvements in the reliability of the transmission lines are demanded for recent transmission apparatuses.

Referring to FIG. 34, the connection setting for line signals VC-n can be freely changed by making a setup change. FIG. 34 shows the concept of a cross connection (line setting) apparatus that has the center role in an exchange system for exchanging time-division signals. As is shown in FIG. 34, a plurality of SDH interface frame signals, called STM-n (Synchronous Transmission Module Level n), are input. Line signals VC-n, which were multiplexed to obtain the STM-n frame signals, are extracted, and output terminals are determined to which VC-n signals are connected across the individual transmission lines. Then, the VC-n signals that have been set as described above are multiplexed again to obtain and output STM-n frame signals.

The STM-n frame signals are multiplexed transmission signals carried on the SDH network, and four different values, 0, 1, 4 and 16, are defined as the values for n at the synchronous transmission module level, the four values corresponding to the synchronous digital hierarchy levels, respectively. STM-1 is a base multiplex unit for the SDH network.

The line signals VC-n correspond to a box, called a virtual container, that is specified to multiplex various items of information as byte units. In addition to VC-4 that has a maximum bit rate of 150 Mbps and a retained information speed of 138 Mbps, there are VC-11, VC-12, VC-2 and VC3, which respectively have speeds corresponding to those for retained information.

Further, in FIG. 34, the connection setting for the VC-n signals can be freely changed by the alteration of the setup.

For a line that has only one output direction but has two input connections, as indicated in FIG. 34 by a solid line and a broken line, the same signal is passed along different routes from a cross connection apparatus at one location. In this case, the solid line indicates an active (ACT) line and the broken line indicates a standby (STB) line, and when deterioration of a signal carried on the ACT line is detected, the connection can be automatically changed to the STB line.

On the other hand, a line having outputs in two directions, relative to an input from one direction, is used to output the same signal in different directions in order to provide a redundant line connection. UNEQ (unequipped) denotes an empty time slot to which a line is not inserted.

As was previously described, to improve a system wherein the lines in a network can be freely changed, and to improve the reliability of the lines, an active and standby line redundancy system is employed for connecting the cross connection (line setting) apparatuses A and B, as is shown in FIG. 35.

In addition, as is shown in FIG. 36, in a RING application, transmission devices A through D having a limited function of line setting, called an Add/Drop multiplex function, are provided with individual line redundancy.

Since the conventional cross connection (line setting) apparatus employs the redundancy method performed across the multiplex STM-n lines, it can cope with the defect between the lines but can not handle a malfunction at the transmission device. Further, as active and standby transmission paths are provided on the same route, when both the active and standby transmission paths may be obstacles at the same time, the reliability of the cross connection apparatus has become low.

In the RING application, line redundancy can be applied only for a limited application, and it is difficult to constitute a line redundancy in a complicated network employing cross connection (line setting) apparatuses.

SUMMARY OF THE INVENTION

It is, therefore, one object of the present invention to provide an exchange system for exchanging time-division signal, while following wired communication system standards as specified by ITU (International Telecommunication Union) or SONET (Synchronous Optical Network), for performing line settings so that when monitoring detects deterioration of signal quality on a line, the transmission line can be easily switched to another line having a different directional orientation.

To achieve the above object of the present invention, a time-division signal exchange system, which receives an SDH interface signal, separates a virtual container line signal that is multiplexed into the SDH interface signal and connects the virtual container line to one of a number of output terminals, comprises:
a signal receiver for receiving a primary signal, for detecting alarm information contained in the primary signal that is received, and for performing conversion of the primary signal in consonance with an occasion when the alarm information is detected;

a signal synchro nizer for, upon receipt of the primary signal and the alarm signal from the signal receiver, switching phases for the primary signal and the alarm information by using a first clock and for outputting the results; and
a TSI function section for exchanging the primary signals received from the signal synchronizer for individual time slots of the primary signals.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a functional block diagram illustrating a line setting apparatus according to the present invention;

FIG. 2 is a functional block diagram illustrating an example arrangement of an input processor;

FIG. 3 is a functional block diagram illustrating the arrangement of an input processor when an input primary signal z-1 is a bipolar signal;

FIG. 4 is a block diagram illustrating an example arrangement of a signal synchronizer;

FIG. 5 is a block diagram illustrating the arrangement of a TSI function unit;

FIG. 6 is a diagram showing an example where a STM-1 signal whose phase is synchronized is mapped in a form STM -1>AU-4>TUG-3>TUG-2>TU-12/TU-2;

FIGS. 7A-7E are diagrams for explaining the process for reading a primary signal (VC-4 signal) from the memory of the signal synchronizer;

FIG. 8 is a block diagram illustrating an example arrangement for a TSI circuit in the TSI function unit;

FIG. 9 is a block diagram illustrating another example arrangement for the TSI circuit in the TSI function unit;

FIG. 10 is a block diagram illustrating an additional example arrangement for the TSI circuit in the TSI function unit;

FIG. 11 is a block diagram illustrating a further example arrangement for the TSI circuit in the TSI function unit;

FIG. 12 is a diagram for explaining the reading of a primary signal from the TSI circuit;

FIG. 13 is a block diagram illustrating an example of a control signal generator;

FIG. 14 are diagrams showing an example where time slots are switched by the TSI circuit;

FIG. 15 is a block diagram illustrating an example arrangement of the control signal generator;

FIG. 16 is a block diagram illustrating an example arrangement of the control signal generator corresponding to FIG. 9;

FIG. 17 is a block diagram illustrating another example of the control signal generator;

FIG. 18 is a diagram illustrating one example of the control signal generator co rresponding to the TSI circuit in FIG. 11;

FIG. 19 is a block diagram illustrating an example arrangement of a transmission signal generator;

FIG. 20 is a block diagram illustrating one user interface;

FIG. 21 is a block diagram illustrating one embodiment of the present invention for performing cross connection (line setting) with STM-4.times.2 lines and STM-1.times.8 lines as input;

FIGS. 22A and 22B are diagrams for comparing a TS I circuit in this embodiment in FIG. 21 with the previously described TSI circuit;

FIG. 23 is a block diagram illustrating example arrangements of line setting circuits in the embodiment in FIG. 21;

FIG. 24 is a time chart (1) for individual signals for the embodiment shown in FIG. 21;

FIG. 25 is a time chart (2) for the individual signals for the embodiment shown in FIG. 21;

FIG. 26 is a diagram illustrating another embodiment for cross connection of STM-4.times.2 lines and STM-1.times.8 lines;

FIG. 27 is a diagram illustrating the arrangement of a line setting circuit used for the embodiment in FIG. 26;

FIG. 28 is a diagram showing a table for explaining the determinations of a selector;

FIG. 29 is a time chart (1) for individual signals for the embodiment shown in FIG. 26;

FIG. 30 is a time chart (2) for the individual signals for the embodiment shown in FIG. 26;

FIG. 31 is a diagram illustrating an additional embodiment where an Add/Drop multiplexer (MUX) is constituted by the line setting circuit shown in FIG. 23

FIG. 32 is a time chart (1) for individual signals for the embodiment shown in FIG. 31;

FIG. 33 is a time chart (2) for the individual signals for the embodiment shown in FIG. 31;

FIG. 34 is a diagram illustrating a conventional cross connection (line setting) apparatus, which serves as the center of a time-division exchange system;

FIG. 35 is a diagram for explaining a current use/spare line redundancy method for the STM-n units; and

FIG. 36 is a diagram for explaining transmission devices in a ring application that have an Add/Drop multiplex line

setting function.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiment of the present invention will now be described while referring to the accompanying drawings. The same reference numerals are used to denote corresponding or identical components in the individual drawings.

FIG. 1 is a functional block diagram illustrating a line setting apparatus according to the present invention. The fundamental functions of the line setting apparatus include:
1) a function for inputting a transmission signal as primary signal (z-1);
2) signal synchronization;
3) a TSI (Time Slot Interchange) function for interchanging time slots;
4) a function for outputting a primary signal (z-2); and
5) a user interface function.

A trunk signal, which is the primary signal, is formed by multiplexing low speed signals as a high speed signal. For example, an STM-1 signal having a transmission speed of 155.52 Mbit/s specified by ITU is formed by multiplexing TU-12 signals having transmission speed of 2.304 Mbit/s for the equivalent of 63 channels.

The TSI processing by a TSI unit 3 is performed to change the constitution of low-speed signals that are multiplexed to obtain a high-speed signal, or to replace a high-speed signal with another high-speed signal. One of the features of the cross connection (line setting) apparatus according to the present invention provides such a TSI function.

The individual functions of the blocks shown in FIG. 1 will be further explained. First, an input processor 1 receives a primary signal z-1 for example, a STM-1 optical signal, detects ALM data, and outputs an alarm (ALM) data signal s-3 to a signal synchronizer 2 across a microcomputer bus s-9. In consonance with an occasion where an ALM has occurred, the input processor 1 converts the primary signal z-1 into an AIS signal and outputs it as a primary signal s-1. The signal s-2, which is also output from the input processor 1, is a clock signal.

The signal synchronizer 2 obtains the phases for the pri s-1 and the ALM data signal s-3 from the signal input processor 1, and exchanges them with those for a clock signal s-6, which is obtained from the TSI unit 3, and outputs the results as signals s-4 and s-5.

The signal synchronizer 2 outputs these signals while aligning the positions of the first bytes of the signals with individual lines called vc (virtual containers). In general, the signal synchronizer 2 also serves as elastic memory and absorbs changes in frequencies that occur between the signal input processor 1 and the TSI unit 3.

The TSI unit 3 replaces the primary signal s-4 from the signal synchronizer 2 in each time slot, and outputs the result as a signal s-7 in a different sequential order. At this time, based on the ALM data signal s-5 and in consonance with the occurrence of the ALM, the contents of the signal s-7 are changed.

At the same time, a clock s-8 is output, which has the same phase as a timing pulse indicating the head of the signal s-7.

An output processor 4 receives the primary signal s-7 and the clock signal s-8, and converts them into an optical signal z-2 that it outputs. Overhead data from a user interface 5 is fetched across a bus interface s-9, and inserted into the primary signal s-7.

The detailed arrangement of the individual functional blocks will now be described.

1) Input processor 1 for inputting a transmission signal as a primary signal z-1:

In order to process a received primary signal z-1, the position of the head of the signal must be determined. First, decoding for example, descrambling of the primary signal z-1 is performed to determine the head position of the primary signal z-1.

The primary signal z-1 includes a special signal indicating the head position e.g., a fixed bit pattern A1 byte, for obtaining frame synchronization, to be inserted into the overhead section of the signal STM-4. This special signal is used to perform synchronization.

The synchronizer 12 performs this synchronization, and is constituted by a counter having a frame cycle and a pattern detector. The positions of various overhead signals and the position of a low-speed signal, which exist in the primary signal z-1, can be specified by the counter. Therefore, the process for extracting individual low-speed signals can be enabled as needed. This process is called demultiplication (DMUX).

The individual overhead data that have been extracted are transferred to an overhead data processor 13, which calculates the data e.g., the counting of the performances of B1, B2 and B3 bytes. The detected ALM is transferred to an ALM processor 11.

The ALM processor 11 collects various signals that are detected by a signal receiver 10, and processes them in the order of their priorities and for example, the ALM processor 11 inhibits synchronous detection of signals when the absence of signals is detected.

As the result of these processes, an ALM data signal a-6 and overhead data signal a-7 are transmitted to the user interface 5 via a bus interface circuit 14.

Sometimes, because of the occurring of an ALM, it is necessary for the primary signal z-1 to be processed to produce a special signal. An AIS process which is performed when reception of an optical signal is halted, is an example process. This process is performed by a signal converter 15. In the AIS process, a signal is masked and is set to "1" in accordance with the occurrence of the ALM.

FIG. 2 is a functional block diagram illustrating the input processor 1. When a received primary signal z-1 is an optical signal, it must be converted into an electric signal. An optical to electrical signal converter 10 performs the conversion of the optical signal to an electrical signal, and the thus produced electrical signal is then output as signal a-1. A clock signal s-2 is also extracted.

FIG. 3 is a diagram illustrating an example arrangement where the received primary signal z-1 is a bipolar signal. In this arrangement, a bipolar signal converter 10 is provided instead of the optical to electrical signal converter 10.

The bipolar signal converter 10 receives an electrical signal z-1-b, which has a bipolar form that is specified by ITU or SONET, and extracts a data element a-1 having a NRZ form and a clock element signal (CLK) s-2 from the electrical signal.

The optical to electrical signal converter 10 in FIG. 2 receives an optical transmission signal z-1 having a form specified by ITU or SONET, and extracts a data element a-1 having a NRZ form and a clock element signal (CLK) s-2 from the optical signal. In addition, the converter 10 detects an ALM data signal a-3 e.g., reception signal level, which indicates there is an abnormality in the received signal, and notifies the ALM processor 11.

Similarly, in FIG. 3, an alarm data signal (ALM) a-3, which indicates that either the input optical signal or the input bipolar signal has a predetermined level or higher, is transferred to an ALM detector 11.

A synchronizer 12 fetches the data element signal a-1 from the optical signal to electrical signal converter 10 or the bipolar converter 10, and extracts a signal a-2 and an a-5 of a low-order group, which is multiplexed in a high-order group. The signal a-2 is transferred to a signal converter 15, and the overhead data signal a-5 is transferred to an overhead data processor 13.

Upon its receipt, the data signal a-5 is processed by the overhead processor 13, i.e., performance data is calculated using B1 byte (Byte) data. Of this data, the ALM data is output as a signal a-4, and the other data is output as a signal a -7. In the arrangement in FIG. 3, the ALM data signal a-4 is transferred directly from the synchronizer 12.

Upon receipt of the signals a-3 and a-4, the ALM processor 11 performs sequential priority order processing of them and outputs a control signal a-8, which serves as a signal conversion trigger for the signal converter 15, and an ALM data signal s-3.

In response to the control signal a-8, the signal converter 15 converts the primary signal a-2 received from the synchronizer 12 into another signal, such as an AIS signal, which is in turn output as a signal s-1.

A bus interface circuit 14 fetches the signals a-6 and a-7 from the ALM processor 11 and the overhead data processor 13, and converts them into bus data signal s-9, which is then output.

2) Signal synchronizer 2

In accordance with clock signal s-6 from the TSI unit 3, the signal synchronizer 2 changes the phases of the primary signal s-1 and the ALM data signal s-3, which have been transferred from the input processor 1, and outputs the results as signals s-4 and s-5. As is shown in FIG. 4, the signal synchronizer 2 is constituted by a memory circuit 20, a signal form converter 21, a memory write circuit 22 and a memory reading circuit 23.

The memory circuit 20, a device for temporarily storing a signal in a matrix form, writes the primary signal s-1 and the ALM data signal s-3, which are received from the input processor 1, in synchronization with a write clock signal b-1 from the memory write circuit 22.

In addition, in accordance with a read clock signal b-2 from the memory read circuit 23, the memory circuit 20 also reads all the stored data, or the data signal (DATA) b-3 in the VC portion and an associated ALM data signal b-4.

If the data signal (DATA) b-3 read from the memory circuit 20 carries all the contents related to the signal s-1, the signals b-3 and b-4 converted from serial to parallel to obtain a form that can easily be handled by the signal form converter 21.

When the read out data (DATA) signal b-3 is a VC, the signal form converter 21 inserts a fixed stuff signal or an overhead signal therein to align the positions of the head bytes for individual channel signals, and outputs the resultant signal as signal s-4.

The timing for the ALM data signal b-4 is adjusted so that its phase matches that of the primary signal s-4, and the adjusted ALM data signal b-4 is output as ALM signal s-5.

3) TSI unit 3:

One example arrangement of the TSI unit 3 is shown in FIG. 5. The TSI unit 3 comprises a TSI circuit 30, a control signal generator 31, a bus interface circuit 32, and an UNEQUIPPED signal generator 33. The TSI circuit 30 stores a received primary signal s-4 in a memory (not shown in FIG. 5) that is a part of the TSI circuit 30. The control signal is read out as a primary signal s-7 in consonance with a control signal c-1 from the control signal generator 31.

At this time, TSI (Time Slot Interchange) is performed by reading signals in a sequential order that differs from the order in which they were input.

The UNEQUIPPED signal generator 33 generates and outputs an UNEQUIPPED signal, so that the UNEQUIPPED signal is also subject to the TSI processing.

To perform the TSI processing, the head positions, at individual levels, of the primary signal s-4, which is input to the TSI unit 3 are determined. First, J1 byte in a virtual container VC-4 having a bit rate of 150.336 Mb/s is set.

FIG. 6 shows a STM-1 signal having a synchronized phase, the signal being mapped in the form STM-1>AU-4>TUG-3>TUG-2>TU-12/TU-2.

*1 in FIG. 6 indicates the mapping position for the overhead of the STM-1, the first byte being defined as an A1 byte. As a result, the pointer byte of TU-3 and V1 byte of TU-2/Tu-12 are positioned at the first row, and the signals for all the hierarchial levels are neatly arranged.

To achieve this arrangement, the VC-4 signal is extracted from the STM-1 signal and is stored in the memory. Re-mapping is performed for this signal at a predetermined timing at which the mapping having the above form is available. This process takes place in the signal synchronizer 2.

The reading out of a primary signal (VC-4 signal) from the memory 20 of the signal synchronizer 2 is correlated with a predetermined timing signal s-6, which is required by the TSI unit 3. Then, the mapping is performed in the signal form as shown in FIG. 6.

This processing is shown in FIG. 7. A STM-1 signal is again stored in the memory of the TSI circuit 30 to perform the TSI process. The STM-1 signal is developed in advance into parallel signals to facilitate its writing to the memory.

Since in the STM-1 signal one byte is the minimum signal unit carrying the meaning, accordingly, the signal is developed into eight parallel signals. This process is performed by the memory reading circuit 23 of the signal synchronizer 2.

To switch the buses, an ALM signal is provided in consonance with the number of bytes. For example, one ALM signal is provided for eight primary signals.

The TSI circuit 30 of the TSI unit 3 is generally constituted as is shown in FIG. 8, or in FIG. 9 to FIG. 11. The arrangement shown in FIG. 8 is employed to perform general processing for a primary signal upon receipt of an input signal s-4. The arrangements in FIGS. 9 through 11 are used to divide a primary signal and to store the divided signals in several memories for processing.

In FIG. 8, the TSI circuit 30 is constituted by two memories 300 and 301 and a signal selector 302. A primary signal s-4 is stored in the two memories 300 and 301, and in accordance with a control signal c-1 from the signal selector 302, it is output as a control signal s-7 in a sequential order that differs from the order in which it was written.

The memories 300 and 301 have sufficient memory capacity to store all of the primary signals and the ALM data received during a cycle T, and are accessible by the control signal c-1.

The primary signal s-4 that is transmitted to the TSI unit 3 is alternately written to the memories 300 and 301. The alternate writing is performed to enable random reading. The data must be read after all of it has been stored in the memories 300 and 301, so that the memories 300 and 301 can act as memories for which reading and writing are constantly performed relative to primary signals that are endlessly received.

More specifically, in consonance with the control signal c-1, the TSI circuit 30 alternately fetches the primary signal s-4 and reads the primary signal s-4 in a changed sequential order in the cycle of 13.89 .mu.s, for example, as is shown in FIG. 12. In response to the control signal c-1, the signal selector 302 selects one of signals c1-1.1 and c1-1.2 that are read from the memories 300 and 301, which are prepared for reading, and outputs the selected signal as a primary signal s-7.

When the selection of the UNEQUIPPED signal is instructed in accordance with the signal c-1, an UNEQUIPPED signal c-4 is selected.

Another arrangement of the TSI circuit 30 shown in FIG. 9 is constituted by 2n memory sets 300-1 through n and 301-1 through n, n signal selectors 302-1 through n, and one signal selector 303.

In an additional arrangement shown in FIG. 10, the TSI circuit 30 has the structure in FIG. 8 for each of primary signals s-4.1 through s-4.n. In addition, a second signal selector 303 and a series/parallel converter 304 are provided.

For an arrangement shown in FIG. 11, a third signal selector 305 is provided to select a primary signal.

In the arrangement for the TSI circuit 30 in FIG. 11, and in addition to the arrangements for the TSI circuit 30 in FIG. 9, a serial/parallel converting circuit 304 is provided at the rear stage of the signal selector 303, and the signal selector 305 is provided behind the serial/parallel converting circuit 304 to switch paths in accordance with a control signal c2-7. The signal selector 305 analyzes the received signals to obtain several primary signals s-7.1 through s-7.m, which are then output.

With the arrangements for the TSI circuit 30 in Figs. 9 through 11, whereby a primary signal is stored in several memories, when the amount of read address data stored in the memory 313 in the control signal generator 31 is increased, and the speed of the read control signal c-1 is accordingly increased, the number of the primary signals s-7 relative to the TSI circuit 30 is also increased.

In FIGS. 9 through 11, the structures of the individual memory sets 300-1 through 300-n and 301-1 through 301-n are the same as those of the memories 300 and 301 in FIG. 8. These memory sets have sufficient memory capacity to store all of the primary signals s-4.n (n through n) and the ALM data received during the cycle T, and can be accessible in accordance with the control signals c-1.n.

The primary signals s-4.n (n=1 through n) are fetched. And the primary signals c1-1.1.1 to c1-1.1.n and c1-1.2.1 to c1-1.2. n are alternately read out, in the sequential order that differs from that in which they were received, in accordance with the control signal c-1.n (c-1 includes CLK signal c-1clk, and ACM data signals c-1.acm1, c-1.acm2 and c-1.sel from the control signal generator, as will be described later).

When the selection of an UNEQUIPPED signal is instructed by the control signal c-1, an UNEQUIPPED signal c-4 is selected.

The signal selectors 302-1 through 302-n receive primary signals c1-1.1.1 through c1-1.1.n and c1-1.2.1 through c1-1.2.n from the memory sets 300-1 through 300-n and 301-1 through 301-n, and select the signals that are ready to be read in accordance with the control signal c-1.sel from the control signal generator 31 (see FIG. 5).

The signal selector 303 selects a signal from the primary signals c1-2.1 though c1-2.n, from the signal selectors 302-1 through 302-n, in accordance with the control signal c-1.sel2 received from the control signal generator 31, which will be described later. The selected signal is output as a primary signal s-7.

The control signal generator 31 of the TSI unit 3 outputs master clock signals s-6.clk, c-1.clk and s-8.clk, which concern the exchange of time slots (signal exchange), and control signals c-1 (c-1.sel, c-1.acm1 and c-1.acm2), which are used to control the TSI circuit 30.

The control signal generator 31 has the arrangement shown in FIG. 13, as an example, and is used together with the TSI circuit 30 in FIG. 8. This control signal generator 31, which has no path switching function, comprises a clock (CLK)

oscillator 310, a pulse generator 311, a control selector 312, a memory 313 and a memory controller 314.

The clock (CLK) oscillator 310 generates master clock signals s-6.clk, c-1.clk and c2-1 concerning the exchange of time slots (exchange of signals). The pulse generator 311 gener ates various timing pulse signals s-6.tp and s-8.tp, which are required for the TSI process, and a control signal c-1.sel, which is relative to the TSI circuit 30.

A data signal c2-4, which is a read addres s signal for the memories 300 and 301 of the TSI circuit 30, is transferred to and stored in the memory 313 by the memory controller 314. This signal is periodically output as a control signal c2-6 in accordance with a control signal c2-2 from the pulse generator 311.

The memory controller 314 fetch es TSI setting data signal c-3 from the bus interface circuit 32 (see FIG. 5), and writes it into the memory 313. The memory controller 314 also outputs data signal c-2, for confirmation of a setting signal, to the bus interface circuit 32, and for confirmation, reads address data from the memory 313.

The control signal selector 312 selects either a write address signal c2-2 from pulse generator 311 or a read address signal c2-6 from the memory 313.

The write address signal c2-2, which is a count-up signal, is an address signal for sequentially writing to the memory 313. In synchronism with the repeated reading and writing relative to the memory 313, the write address signal c2-2 and the TSI control signal c2-6 are alternately selected by the control signal selec tor 312, and are output as control signals c-1.acm1 and c-1.acm2.

The cycle for reading/writing the memory 313 is a time period (125/9 .mu.s) required for one row. Since the STM-1 signal has the same signal arrang ement for each row, as is shown in FIG. 6, only data for one row need be fetched to adequately perform TSI.

When the signal format is restricted, data for even 1/4 row enables the TSI process. Once the data has been stored in the memory they can be read at random while being output. This property is employed to implement the TSI function. As is shown in FIG. 14, for example, by comparing the memory input time with the memory output time, columns 100 and 101 are ex changed

When a plurality of memories 313 are provided, they can be selected by a selector. Also, available for switching paths there are a m ethod for selecting a memory control signal according to ALM data and a method for selecting a primary signal after the TSI.

According to the method for selecting the memory control signal, data for signals to be selected when an A LM occurs are stored in advance in memories 313-1 and 313-2, as is shown in an example arrangement for the control signal generator 31 in FIG. 15.

In addition, a signal discriminator 316 and a second control signal selec tor 315 are pro vided to select one of the outputs of the memories 313-1 and 313-2 in consonance with the situation during which the ALM has occurred. Since a control signal is changed in consonance with the situation during which the ALM has occurred, a primary signal is accordingly altered.

The example of the control signal generator 31 in FIG. 15 corresponds to the TSI circuit 30 in FIG. 8, but has a path switching function. The control signal generator 31 comprises a CLK oscillator 310, a pulse gener ator 311, a control signal selector 312, memories 313 -1 and 313-2, a memory controller 314 and a signal discriminator 316.

The control signal genera tor 31 generates master clock signals (CLKS) s-6.clk, c-1.clk and s-8.clk concerning cross connections (signal exchanges). Further, the control signal generator 31 out puts timing pulse signals s-6.tp and s-8.tp for controlling t he block timing, and control signals c-1 (c-1.sel, c-1.acm1 and c-1.acm2) for controlling the TSI circuit 30.

The difference between this arrangement and the arrangement for the control signal generator 31 in FIG. 13 is that an ALM data signal s-5 is received, and in accordance with this, the contents of the control signals c-1.acm1 and c-1.acm2 for controlling t he memories 300 and 301 of the TSI circuit 30 are change d.

Moreover, in FIG. 15, in addition with the arrangement of the TSI circuit 30 in FIG. 8, data signals c2-4.1 and c2-4.2, which serve as read addres s signals for the memories 300 and 301, are transferred to and stored in t he memories 313 - 1 and 313-2 by the memory controller 314. These signals are periodic ally output in accordance with the control signal c2-2 from the pulse generator 311.

In FIG. 15, as the number of t he memories corresponding to those in the TSI circuit 30 is increased, signals output from the memory controller 314 are increased to c2-4.1 and c2-4.2, and input signals are increased to c2-5.1 and c2-5.2.

The signal discriminator 316 output s a selection signal for selecting one of the memories 313-1 and 313-2 based on a line ALM signal s-5 from the signal sy nchronizer 2. The control signal selec tor 312 selects one of the read address signals output from the memories 313-1 and 313-2 in consonance with the control signal c2-7 from the signal discriminator 316.

According to the arrangement in FIG. 15, the control signal selector 312 selects the write address signal c2-2 output from the pulse generator 311 and the signal c2-6.c output from the selector 315.

In FIG. 16 is shown a control signal genera tor 31 corresponding to FIG. 9. This control signal generator 31 does not have the path switching function, and includes a CLK oscillator 310, a pulse generator 311, a control signal selector 312, a memory 313 and a m emory controller 314.

The control signal genera tor 31 in FIG. 16 generates master clock signals (CLKS) s-6.clk, c-1.clk and s-8.clk concerning the exchange of t he time slots (signal exchange). The control signal gener ator 31 also outputs timing pulse signals s-6.tp and s-8.tp for controlling the timing for blocks, and also control signals c-1 (c-1.sel, c-1.acm1, c-1.acm2 and c-1.sel2) for controlling the TSI circuit 30.

A data signal c2-4, which serves as a read address signal for the memories 300 and 301, is transferred and stored in the memory 313 by the memory controller 314, and is periodically output as a control signal c2 -6 in consonance with a control signal c2-2 from the pulse generator 311. When this signal is used by the TSI circuit 30 in FIG. 9, the signal c-1.sel2 for controlling the signal selec tor 303 of the TSI circuit 30 is also output.

A control signal generator 31 having the arrangement in FIG. 17 corresponds to the TSI circuit 30 in FIG. 9, but has the path switching function. The control signal generator 31 in FIG. 17 includes a CLK oscillator 310, a pulse generator 311, a control signal selector 316, memories 313-1 and 313-2, a memory controller 314, a signal discriminator 315 and a control signal selector 312.

The control signal generator 31 in FIG. 17 generates clock signals (CLKS) s-6.clk, c-1.clk and s-8.clk, which are master clocks related to signal exchange, also outputs timing pulse signals s-6.tp and s-8.tp for controlling the timings of blocks.

The control signal generator 31 also outputs control signals c-1 (c-1.sel, c-1.acm1, c-1.acm2 and c-1.sel2) for controlling the TSI circuit 30.

The difference between this generator and the control signal generator 31 in FIG. 16 is that an ALM data signal s-5 is received, and in accordance with this data, the contents of the control signals c-1.acm1, c-1.acm2 and c-1.sel2 for controlling the memories 300 and 301 of the TSI circuit 30 are changed.

In FIG. 18 is shown an example control signal generator that corresponds to the TSI circuit 30 in FIG. 11. In addition to the arrangement shown in FIG. 16, a signal discriminator 315 is provided to receive an ALM data signal s-5 and output a control signal c2-7.

4) Transmission signal generator 4:

FIG. 19 is a diagram illustrating an example arrangement for the transmission signal generator 4 (see FIG. 1). The transmission signal generator 4 compris es a memory circuit 40, a memory reading circuit 41, an overhead byte insertion circuit 42, a signal multiplexer 43, a signal converter 44 and a bus interface circuit 45.

The transmission signal generator 4 receives a primary signal s-7, a clock signal s-8.clk and a timing pulse signal s-8.tp from the TSI unit 3 and converts them into an optical signal z-2, which is then output.

At this time, the transmission signal generator 4 fetches overhead data from the user interface unit 5 via the bus interface s-9, and inserts it into the primary signal s-7.

The memory circuit 40 fetches and stores the primary signal s-7 input by the TSI unit 3. Further, in accordance with a read clock signal d-1 from the memory reading circuit 41, the memory circuit 40 outputs the stored data.

The memory reading circuit 41 receives the clock signal s-8.clk and the timing pulse signal s-8.tp from the TSI unit 3, and outputs the read clock signal d-1 for controlling the reading of the memory circuit 40.

The overhead byte insertion circuit 42 fetches a primary signal d-2 read from the memory circuit 40, and inserts overhead data into a predetermined time slot. At this time, the overhead byte insertion circuit 42 also fetches overhead data d-3 from the bus interface circuit 45, and inserts it into the predetermined time slot.

The signal multiplexer 43 performs serial/parallel conversion of a primary signal d-4 received from the overhead byte insertion circuit 42 so as to obtain a suitable signal form for the signal converter 44. At this time, the signal multiplexer 43 also performs a coding process, such as scrambling.

The signal converter 44, which has the electrical to optical signal conversion function, converts a primary signal d-5 from the signal multiplexer 43 into an optical signal z-2 e.g., STM-1 signal, which is output.

The bus interface circuit 45 is connected to the user interface unit 5 by a bus for the transmission of overhead data signal d-3 that is designated by a user for the overhead byte insertion circuit 42.

Instead of being as an electrical to optical signal converter, the signal converter 44 can be an output circuit for outputting a bipolar signal, which is an electrical signal.

The signal converter 44, which functions as an output circuit for a bipolar signal, outputs a signal from the signal multiplexer 43 as, for example, an electrical signal of 140 Mbps.

The primary signal output by the TSI unit 3 is transferred to the memory 40 in the signal generator 4. This occurs because the primary signal is changed to a clock signal source that differs from that of the CLK oscillator 310 of the TSI unit 3 but is synchronized with the CLK oscillator 310.

At this time, an AU-4 pointer is replaced. Further, the overhead data is inserted into a specific position in the primary signal by the overhead byte insertion circuit 42. Also inserted is the data for a client setup, which is received from the bus interface circuit 45 that is connected to the user interface unit 5.

Following this, serial/parallel conversion is performed for the primary signal to acquire the form of a signal that is appropriate for the signal converter 44. At this time, coding (scrambling) of the primary signal, disabling of parity, and the insertion of a B1 Byte, etc., are also performed.

Finally, the resultant signal is converted into an optical signal z-2 by the signal converter 44, and the optical signal z-2 is output.

5) User interface function:

The functions of the user interface unit 5 are the processing of ALM data for a received primary signal, the display of performance data and overhead data on a display or a terminal, the calculation by a computation circuit of line data for client setup, the transmission of the result to the TSI unit 3 by using a bus signal, and the transmission of the overhead data for client setup to the signal generator 4.

More specifically, the user interface unit 5 performs an intermediate process for transmission the setting performed by a user to the signal receiver 1, the TSI unit 3 or the signal generator 4 across the bus s-9, or for displaying the state (ALM, etc.) of a received primary signal and the overhead data included in that signal.

An example of the user interface unit 5 is shown in FIG. 20. The user interface unit 5 comprises a bus controller 50, a

memory 51, a CPU 52 and an external interface circuit 53.

The bus controller 50 is connected to the signal input processor 1, the TSI unit 3 or the bus interface circuit of the signal generator 4 across the bus s-9 for the exchange of ALM data and overhead data.

In the memory 51 are stored line setting data designated by a user, ALM data collected on the overhead or the input signal processor 1, and temporary data used by the CPU 52 for computation.

The CPU 52 is connected to the bus controller 50, the memory 51 and the external interface circuit 53, and changes the format of the input/output data by performing computation.

The external interface circuit 53 has interface ports for various devices e.g., a display device, a keyboard and a portable terminal to provide an interface with a user. The external interface circuit 53 transfers data from these devices to the CPU 52 and outputs various data stored in the memory 51 via the CPU 52 from the interface ports.

FIG. 21 is a diagram illustrating one embodiment , of the present invention, described above in detail, for performing a cross connection (a line setting) while inputting STM-4.times.2 lines and STM-1.times.8 lines.

In FIG. 21, the diagrams used for the above description are partially simplified and the sequential order of the connections is changed. As is shown in FIG. 21, two STM-4 signals and eight STM-1 signals are input to a signal input processor 1, and are converted into electric signals by an optical to electrical signal converter 10 in the signal input processor 1.

The STM-1 signals are multiplexed in the STM-4 signal, and ALM processors 11 in the signal input processor 1 process ALM monitor signals by using a STM-1 level signal in common. Therefore, the STM-4 signal is divided into four STM-1 signals by a synchronizer 12 of the signal input processor 1.

Since the STM-n signals that are input to the cross connection (line setting) apparatus each have different frame timings, their time slot positions must be aligned to perform cross-connection.

Thus, the write and read timings relative to the memory 20 of the signal synchronizer 2 shown in FIG. 4 are controlled, and the frame timing positions of all the input STM-1 signals are adjusted so that they match each other.

The ALM processor 11, which processes an ALM monitor signal, monitors each channel of the ALM (alarm) state for VC-n signals that are multiplexed into each input STM-1 signal.

In consonance with the ALM state that is monitored, a signal indicating the state of each channel signal, SF (Signal fail), SD (Signal degrade) or NO-ALM, is output.

Then, Upon receipt of the primary signal data and the alarm signal, a signal converter 21 of the signal synchronizer 2 multiplexes the STM-1 signal to obtain an STM-4 signal, so that line setting is facilitated. The resultant signal STM-4 is transferred to a TSI unit 3.

A UNEQ signal generator 33 in the TSI unit 3 generates an STM-4 signal obtained by multiplexing VC-12 UNEQUIPPED signal by the equivalent of 252 channels. A TSI circuit 30 in the TSI unit 3 includes line setting circuits 131 to 164.

When the TSI circuit 30 in the embodiment in FIG. 21 is compared with the previously described TSI circuit examples 30, this corresponds to the one specifically shown in FIGS. 22A and 22B. That is, the structure in FIG. 22A corresponds to the arrangement of the TSI circuit 30 described previously, where line setting elements 100 correspond to the assembly composed of the memories 300 and 301 and the signal selector 302. A selector 101 corresponds to the selector 303 (see FIG. 9).

The outputs of the line setting elements 100 are collectively transferred to the selector 101, which selects one of these outputs.

On the other hand, in the embodiment shown in FIG. 21, as is shown in FIG. 22B, each of the line setting elements 131 through 164, which are each constituted by a line setting element 100 and a selector 102, are cascaded.

In the embodiment in FIG. 21, a total of 16 line setting elements are provided because one set of each vertically arranged four elements implements the TSI for an STM-4 (total of four sets corresponds to an STM-16). One set of vertical elements can not implement the TSI for an STM-16 because the speed of the device is limited. Therefore, the speed is reduced to 1/4, while the size of the line scale is increased four times.

The quantity of data processed by the TSI circuit 30 can be varied depending on the address speed. When the address speed is set equivalent to an STM-16, one set of the line setting elements in FIG. 21 is sufficient.

In the embodiment in FIG. 21, an arbitrary VC-n signal for an STM-4 signal received from the signal converter 21 is inserted into a through signal transferred from the UNEQ signal generator 33 or the upper-level line setting circuit. At this time, line setting is also performed for a condition signal that is added to the VC-n.

Further, line selectors (path switch: PW) 140 and 141 are provided to select one of the signals, which are cross connected by the line setting circuits 131 through 164, in consonance with the condition signals that are added to the VC-n.

For a channel for which no redundancy processing is performed, the signals are output without a selection being made. With this arrangement, since the connections of the line setting elements are increased vertically at many stages, the capacity of input signals is increased. When the connections of the line setting elements are increased horizontally at many stages, the capacity of output signals is increased. Thus, as the whole, the line setting capacity can be easily increased.

An example arrangement of each of the line setting circuits 131 through 164 in the embodiment in FIG. 21 is shown in FIG. 23. The line setting element 100 is constituted by a data memory. The data memory 100 has two sides, each having sufficient memory capacity to hold STM-4 signals for one row (125/9 .mu.s) and a three-bit ALM signal.

Each side has a one-row memory capacity because the repeating of channels is performed for each row. While signals

are written on one side, from the left in the input order, data for an immediately preceding row are written on the other side, and arbitrary data are read from the address memory 103 in consonance with an address. In this manner, the writing and the reading are changed for each row.

Input source data for each data byte in one row of signals that is to be output is held in the address memory 103. The following input source data are stored in the memory and can be rewritten externally:
(1) whether data is from a through input or is read from the data memory 100; and
(2) an address for data to be read from the data memory 100.

The output of the data memory and the through data are transferred to the selector 102. In consonance with the contents of the address memory 103, either through data or the data from the data memory 100 is selected. Before this selection, the frame timing positions of both data should be matched.

The time chart for individual signals in the embodiment in FIG. 21 is shown in FIGS. 24 and 25. Reference numerals in parentheses in FIG. 24 correspond to those in FIG. 21.

FIG. 26 is a diagram for another embodiment, which is a path switching example where a memory control signal is selected in consonance with ALM data. As well as in FIG. 21, STM-4.times.2 and STM-1.times.8 are employed as input to perform cross connections.

As is in the embodiment in FIG. 21, arbitrary VC-n of multiplexed STM-4 signals are inserted into through signals sent from the UNEQ generator or from the line setting circuits. At this time, line setting is also performed for condition signals added to the VC-n.

At a set time slot, an ALM of a signal from an upper level and an ALM of a signal to be inserted are monitored and the signal having the better quality is selected. Thus, the redundancy function can be provided.

FIG. 27 is a diagram illustrating the arrangement of a line setting circuit used for the embodiment in FIG. 26. The difference between this circuit and the line setting circuit in FIG. 23, used for the embodiment shown in FIG. 21, is that a selector discriminator 104 is provided. The selector discriminator 104 corresponds to the control signal selector 312 and the discriminator 315 (see FIG. 17, for example), both of which were previously described.

A data memory 100 has two memory sides, each having sufficient capacity to hold one row (125/9 .mu.s) of STM-4 signals and a three-bit ALM signal.

Each side has a memory capacity sufficient for one row because the repeating of channels is performed for each row. While signals are written on one side from the left in the sequential input order, data for an immediately preceding row are written on the other side, and arbitrary data are read in consonance with an address from an address memory 103. In this manner, the writing and the reading are changed for each row.

Input source data for each data byte for one row of signals to be output, and data for determining whether redundancy processing should be performed are held in the address memory 103. The data in the memory can be rewritten externally. The following input source data are stored:
(1) whether data is from a through input or is read from the data memory 100;
(2) addresses of data to be read from the data memory 100; and
(3) whether or not a time slot for that data should be redundant.

The selector discriminator 104 employs the data (1) and (3) from the address memory 103 and ALM data from the signals to determine whether the through data or data from the data memory 100 should be selected. The contents of the determination are shown in FIG. 28.

In response to the result of the determination performed by the selector discriminator 104, the selector 102 selects either the through data or the data from the data memory 100 in consonance with the contents of the address memory 103. For the selection, the frame timing positions of both data must be matched.

The time chart for individual signals in the embodiment in FIG. 26 is shown in FIGS. 29 and 30. Reference numerals in parentheses in FIG. 29 correspond to those in FIG. 26.

An Add/Drop multiplexer (MUX) can be arranged as shown in FIG. 31 by using the line setting circuit in FIG. 23. The Add/Drop MUX is a multiplexer by which unidirectional low-order group of signals is interfaced, relative to a bidirectional high-order group of signals, and for which a cross connection function is limited.

With this limitation, the exchange of time slots is inhibited for a connection between high-order signal groups. For a connection between a high-order and a low-order group, time slots can be switched freely. The time chart of individual signals in this embodiment in FIG. 31 is shown in FIGS. 32 and 33. Reference numerals in parentheses in FIG. 32 correspond to those in FIG. 31.

As is described above in the embodiments, according to the present invention, a large-scale line setting function can be provided. Since high reliability for the line setting is obtained, the line redundancy function and an efficient circuit structure can be acquired. Therefore, a circuit structure can be provided where the setting for the validity and the invalidity of the line setting function is flexible and efficient.

In addition, an Add/Drop MUX device can be arranged by using the same line setting circuit.

The above explained embodiments and drawings are used only for explaining the present invention, and therefore, the present invention is not restricted to the embodiments and drawings. The protective scope of the present invention is determined by the description of the attached claims, and the equivalents to the claims are within the scope of the present invention.

Cross connection system for time-division multiplexed signal

Claims not available for **CN 1177246 (A)**
Claims of corresponding document: **US 6034947 (A)**

What is claimed is:

1. A cross-connecting system for receiving an SDH interface frame signal, separating a virtual container line signal that is multiplexed into said SDH interface signal and connecting said virtual container line signal to one of output terminals, comprising:
a signal receiver receiving primary signals, detecting alarm information contained in said primary signals, and performing conversion of said primary signals in consonance with occasions when said alarm information is generated;
a signal synchronizer receiving said primary signals and said alarm information from said signal receiver, and switching respective phases of said primary signals and said alarm information to phases based on one common clock; and
a TSI function section exchanging time slots of said primary signals output from said signal synchronizer and outputting said primary signals having exchanged time slots.

2. The cross-connecting system according to claim 1,
wherein said one common clock is output from said TSI function unit.

3. The cross-connecting system according to claim 1,
wherein said TSI function unit includes a memory storing said primary signals, and said primary signals are read from said memory in a sequential order that differs from that in which said primary signals have been written to said memory, so that time slots of said primary signals are exchanged.

4. The cross-connecting system according to claim 1,
wherein said TSI function unit has two memories storing said primary signals, and a signal selector selecting to read said primary signals out from said memories, alternately.

5. The cross-connecting system according to claim 1,
wherein said TSI function unit includes n sets of two memories storing said primary signals, n signal selectors each for controlling the two memories to output said primary signals, alternately, and an output selector for selecting one of said n signal selectors to output primary signals out from the two memories controlled by the selected one of the n signal selectors.

6. The cross-connecting system according to claim 1, further comprising a signal generator including a memory storing an output of said TSI function unit, and an overhead data insertion circuit inserting overhead data into data read out from said memory.

7. The cross-connecting system according to claim 6,
wherein said primary signal is an optical signal, said signal receiver includes an optical to electrical signal converter, and said signal generator includes an electrical to optical signal converter.

8. The cross-connecting system according to claim 6,
wherein said primary signal is an STM-n signal, said signal receiver includes a circuit demultiplexing said STM-n signal into a plurality of STM-1 signals, and said signal synchronizer synchronizes phases of said plurality of STM-1 signals.

9. Across connection system for time-division multiplexed signals comprising:
first means for demultiplexing an input STM-n signal into a plurality of STM-1 signals;
second means for adjusting phases of said plurality of STM-1 signals to match frame timing positions;
third means for monitoring, for each channel, alarm conditions of VC-n signals which are multiplexed with said plurality of STM-1 signals, and for adding a signal identifying said monitored alarm condition to said signals of which said phases have been adjusted by said second means;
fourth means for generating STM-n signals with which VC-12 UNEQ signals are multiplexed; and
fifth means for inserting an arbitrary VC-n of a lower output from said third means into an upper output from said third means or into an output from said fourth means.

10. The cross connection system according to claim 9,
wherein said fifth means includes line selection means for selecting either one of two signals cross-connected according to a condition signal, which is added to said VC-n signal provided in said two signals.

11. The cross connection system according to claim 10,
wherein for a set time slot, an alarm for a signal sent from an upper level is compared with an alarm for a signal to be inserted, and the signal having a higher quality is selected.

12. The cross connection system according to claim 9,
wherein said fifth means includes a data memory having two sides of capacities adequate for storing one row of STM-n signals and an alarm signal; an address memory storing input source data for each byte of data for one row, which is to be output from said data memory; and a selector selecting either a UNEQ signal, or data read out from said data memory, in consonance with contents of said address memory.

13. The cross connection system according to claim 12,
wherein said input source data stored in said address memory includes information concerning whether said input source data is a UNEQ signal or data read from said data memory, and addresses of data to be read from said data memory; wherein in said address memory is stored data for determining whether or not a time slot is used for redundancy; and wherein a selector discriminator is provided controlling a selection by said selector by using information concerning whether data is through input data or data read from said memory, information for determining whether or not said time slot in said address memory is used for redundancy, and alarm information for each signal.

14. The cross connection system according to claim 9,
wherein said STM-n signals are STM-4 signals.

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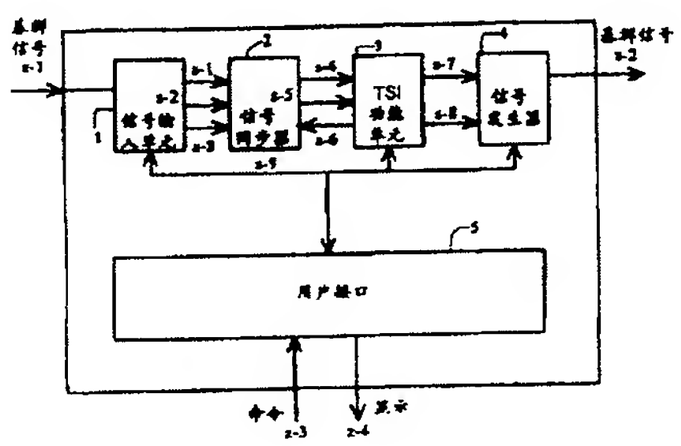
[54]发明名称 时分复用信号的交叉连接系统

[57]摘要

一种用于时分复用信号的交叉连接系统，当检测到质量恶化时进行线路配置，以易于切换到含另一方向定位的线路。该交叉连接系统接收 SDH 接口信号，把复用到 SDH 接口信号中的虚容器线路信号分开，并把该虚容器线路连到若干输出终端中的一个。该交叉连接系统包括一个用于接收一种基准信号的信号接收器；一个信号同步器；以及一个 TSI 功能部分。



权　利　要　求　书

1.一种用于接收时分复用信号的交叉连接系统，它接收SDH接口信号，把复用到所述的SDH接口信号的虚容器线路信号分开，并且把所说的虚容器线路信号连接到多个输出终端之一，包括：

一个用于接收基群信号的信号接收器，用于检测在所述的基群信号中包含的告警信息，以及在检测到所述的告警信息时进行该基群信号的变换；

一个信号同步器，用于当从所述的信号接收到所述的基群信号和告警信号时，通过利用第一时钟对该基群信号和该告警信号改变相位，并且用于输出该结果；以及

一个TSI功能部分，用于对从所述的信号同步器输出的所述的基群信号的各个时隙进行交换，并且输出该已交换时隙的基群信号。

2.根据权利要求1的交叉连接系统，其特征在于其中所述的第一时钟从所述的TSI功能单元输出。

3.根据权利要求1的交叉连接系统，其特征在于其中所述的TSI功能单元包括一个用于存贮所述的基群信号的存贮器，并且该基群信号按不同于该基群信号写入所述的存贮器的一种序列顺序，从该存贮器读取，使得对于每一时隙该基群信号得到交换。

4.根据权利要求1的交叉连接系统，其特征在于其中所述的TSI功能单元含有用于存贮所述的基群信号的两个存贮器，以及一个用于交替地选择从所述的两个存贮器读出该基群信号的信号选择器。

5.根据权利要求1的交叉连接系统，其特征在于其中所述的TSI功能单元包括：用于存贮所述的基群信号的n组的两个存贮器；各用于交替地控制两个存贮器以输出该基群信号的n个信号选择器；以及一个输出选择器，该输出选择器用于选择所述的n个信号选择器之一，以输出来自由所选的n个信号选择器之一控制的两个存贮器的基群信号。

6.根据权利要求1的交叉连接系统，其特征在于还包括一个信号发生器，后者包括一个用于存贮所述的TSI功能单元的输出的存贮器，以及一个把开销数据插入到从该存贮器读出的数据之中的开销数据插入电路。

7.根据权利要求6的交叉连接系统，其特征在于其中所述的基群信

号是一种光信号，所述的信号接收器包括一个光/电信号转换器，并且所述的信号发生器包括一个电/光信号转换器。

8.根据权利要求 6 的交叉连接系统，其特征在于其中所述的基群信号是一种 STM - n 信号，所述的信号接收器包括一个用于把所述的 STM - n 信号解复用成多个 STM - 1 信号的电路，并且所述的信号同步器对所述的多个 STM - 1 信号的相位进行同步。

9.一种用于时分复用信号的交叉连接系统，包括:

第一装置，用于把一种输入的 STM - n 信号解复用成为多个 STM - 1 信号;

第二装置，用于调节所说的多个 STM - 1 信号的相位，以使各帧定时位置相一致;

第三装置，用于对每一信道的复用成所述的多个 STM - 1 信号的 VC - n 信号的告警状态进行监控，以及用于把一种识别所述的受监控告警状态的信号加到其所述的相位已由所述的第二设备调节的所述信号上;

第四装置，用于产生用以使 VC - 12 UNEQ 信号进行复用的 STM - n 信号；以及

第五装置，用于把来自所述的第三装置的较高级输出的一种任选 VC-n 插入到来自该第三装置的较低级输出中或插入到来自所述的第四装置的输出中。

10.根据权利要求 9 的交叉连接系统，其特征在于其中所述的第五装置包括线路选择装置，用于根据一种状态信号选择交叉连接的两种信号的任何一种，该状态信号加到所述的两种信号中提供的所述的 VC - n 信号上。

11.根据权利要求 11 的交叉连接系统，其特征在于对于一设定时隙，将从较高级发送的一种信号告警与要插入的一种信号告警进行比较，并且选出具有较高质量的信号。

12.根据权利要求 9 的交叉连接系统，其特征在于其中所述的第五装置包括: 一个数据存贮器，它含有两面的容量，足够用于存贮一行 STM - n 信号和一个告警信号; 一个地址存贮器，用于对要从所述的数据存贮器输出的一行的各数据字节的输入源数据进行存贮; 以及一个选择器，用于根据所述的地址存贮器的内容，选择一种 UNEQ 信号或从该数

据存贮器读出的数据。

13.根据权利要求 12 的交叉连接系统，其特征在于其中存贮在所述的地址存贮器中的所述的输入源数据包括有关输入源数据是一种 UNEQ 信号还是从所说的数据存贮器读出的数据的信息，以及要从该数据存贮器读取的数据的地址的信息；其中在所述的地址存贮器中存贮用于确定是不是一个时隙用于冗余的数据；并且其中设置一个选择鉴别器，用于控制由所述的选择器作的选择，在此，该选择器是通过利用：有关数据是直通数据还是从所述的存贮器读取的数据的信息、用于确定是不是在所述的地址存贮器中的所述时隙用于冗余的信息、以及用于各信号的告警信息来进行所述选择的。

14.根据权利要求 9 的交叉连接系统，其特征在于其中所述的 STM - n 信号为 STM - 4 信号。

说　　明　　书

时分复用信号的交叉连接系统

本发明涉及一种用于时分复用信号的交叉连接（线路配置，即 line-setting）系统，而且特别是涉及在用于交换为 SDH（同步数字体系）网络而提供的时分复用信号的交换系统中包括通道交换的交叉连接系统。

SDH 技术是一种国际标准化的复用方法，它能有效地应用于电话业务和传输文本数据和图像数据的其他业务。

与在有关交叉连接（线路配置）设备的技术方面已经取得的进展一致，对于新的传输设备，要求系统中整个网络的传输线路可自由地加以改变，并且在传输线路的可靠性方面有改善。

参照图 34，对线路信号 VC-n 的连接配置可通过改变设置自由地加以改变。图 34 表示一种交叉连接（线路配置）设备的概念，这种交叉连接设备在用于交换时分信号的交换系统中具有核心作用。如图 34 所示，被称为 STM－n（同步传输模块等级 n）的多个 SDH 接口帧信号，为输入信号。经复用以得到 STM－n 帧信号的线路信号 VC－n 被提取，并确定输出端跨过各个传输线路与哪些 VC－n 信号相连接。然后，如上所述经设置的 VC－n 信号再一次经复用得到 STM－n 帧信号并输出。

STM-n 帧信号是在 SDH 网络上传送的经复用的传输信号，而四种不同的值，0、1、4 和 16，定义为同步传输模块等级 n 的值，这四种值分别对应于同步数字体系的等级。STM－1 是用于 SDH 网络的基本复用单元。

线路信号 VC-n 对应于一个“箱”（Box），称为虚容器，它被指定以字节单元的形式复用各种信息项。除了 VC-4 含有 150Mbps 的最大比特率以及 138Mbps 的被保留的信息速率之外，还有 VC-11，VC－12、VC－2 以及 VC－3，这些速率分别对应于相应的保留的信息的速率。

此外，在图 34 中，对于 VC-n 信号的连接配置可通过设置的变换而自由地加以改变。

对于一条只有一个输出方向但有两个输入连接的线路，如图 34 由

一条实线和一条虚线所表示，同样的信号经过同一位置的交叉连接设备的不同路由进行传送。在这种情况下，实线表示现用（ ACT ）线路而虚线表示备用（ STB ）线路，并且当检测到 ACT 线路上运送的信号恶化时，连接可自动地变换到 STB 线路。

另一方面，相对于来自一个方向的输入，一条含有以两个方向输出的线路用来按不同的方向输出同一信号以提供冗余线路连接。 UNEQ（未装备）表示没有插入线路的一个空时隙。

如前所述，为改善系统使其在网络中的线路可自由地加以改变，并且为改善线路的可靠性，使用一种现用和备用线路冗余系统用于连接交叉连接（线路配置）设备 A 和 B，如图 35 所示。

除此以外，如图 36 所示，在环形应用中，含有受到限制的线路配置功能称为插/分复用功能的传输设备 A 至 D，备有各个线路的冗余。

由于通用的交叉连接（线路配置）设置使用由复用 STM － n 线路执行的冗余方法，它能处理线路之间的故障但不能处理在传输设备中的故障。此外，由于现用和备用传输通道设置在相同的路由上，所以如果现用和备用传输通道两者可能在同一时刻受到阻碍，交叉连接设备的可靠性就会变低。

在环形应用中，线路冗余只能适用于有限的应用，并且在一个使用交叉连接（线路配置）设备的复杂网络中难于构成线路冗余。

因此，本发明的一个目的是在按照由 ITU （国际电信联盟）或 SONET （同步光网络）所规定的有线通信系统标准的同时，提供一种用于交换时分信号的交换系统，用于完成线路配置，以便当监视检测到一条线路上的信号性能的恶化时，该传输线路可容易地切换到另一条由不同方向来的线路。

为实现本发明的上述目的，一种时分信号交换系统，它接收 SDH 接口信号，把复用到 SDH 接口信号中的虚容器线路信号分开，并且把虚容器线路连接到多个输出终端之一，该时分信号交换系统包括:

一个用于接收基群信号（ primary signal ）的信号接收器，用于检测在所接收的基群信号中包含的告警信息，以及用于在检测到告警信息时进行基群信号的变换;

一个信号同步器，用于当从信号接收器收到基群信号和告警信号时，通过利用第一时钟对基群信号和告警信息改变相位，并且用于输出

该结果；以及

一个 TSI（时隙交换）功能部分，用于对从信号同步器接收的基群信号对于基群信号的各个时隙进行交换。

图 1 是说明按照本发明的一种线路配置设备的功能框图；

图 2 是说明输入处理器的一种配置实例的功能框图；

图 3 是说明当输入基群信号 Z－1 为双极性信号时的一种输入处理器的配置的功能框图；

图 4 是说明信号同步器的一种配置实例的框图；

图 5 是说明一个 TSI 功能单元的配置的框图；

图 6 是表示其相位经同步的 STM－1 信号以 STM－1>AU-4>TUG-3>TUG-2>TU-12/TU－2 的形式映射的一种实例的示意图；

图 7A－7E 是用于说明从信号同步器的存贮器中读取基群信号（VC－4 信号）的过程的示意图；

图 8 是说明 TSI 功能单元中的 TSI 电路的一种配置实例的框图；

图 9 是说明 TSI 功能单元中的 TSI 电路的另一种配置实例的框图；

图 10 是说明 TSI 功能单元中的 TSI 电路的一种另外的配置实例的框图；

图 11 是说明 TSI 功能单元中的 TSI 电路的另一种配置实例的框图；

图 12A－12C 是说明从 TSI 电路读取基群信号的示意图；

图 13 是说明一种控制信号发生器实例的框图；

图 14A 和 14B 是表示通过 TSI 电路进行时隙交换的一种实例的示意图；

图 15 是说明控制信号发生器的一种配置实例的框图；

图 16 是说明对应于图 9 的控制信号发生器的一种配置实例的框图；

图 17 是说明控制信号发生器的另一种实例的框图；

图 18 是说明对应于图 11 中的 TSI 电路的控制信号发生器的一种实例的框图；

图 19 是说明传输信号发生器的一种配置实例的框图；

图 20 是说明一种用户接口的框图；

图 21 是说明用于完成具有 STM－4×2 线和 STM－1×8 线作

为输入的交叉连接（线路配置）的本发明的一种实施方案的框图；

图 22A 和 22B 是把在图 21 的这种实施方案中的 TSI 电路与前面所述的 TSI 电路进行比较的示意图；

图 23 是说明在图 21 的实施方案中线路配置电路的配置实例的框图；

图 24 是图 21 所示的实施方案的各个信号的时序图（ 1 ）；

图 25 是图 21 所示的实施方案的各个信号的时序图（ 2 ）；

图 26 是说明用于 STM － 4 × 2 线和 STM － 1 × 8 线的交叉连接的另一种实施方案的示意图；

图 27 是说明用于图 26 中的实施方案的线路配置电路的配置示意图；

图 28 是表示用于说明选择器的判决的一种表格图；

图 29 是图 26 所示的实施方案的各个信号的时序图（ 1 ）；

图 30 是图 26 所示的实施方案的各个信号的时序图（ 2 ）；

图 31 是说明另一种由图 23 所示的线路配置电路构成的插/分复用器的实施方案的示意图；

图 32 是图 31 所示的实施方案的各个信号的时序图（ 1 ）；

图 33 是图 31 所示的实施方案的各个信号的时序图（ 2 ）；

图 34 是说明一种通用的交叉连接（线路配置）设备的示意图，该设备起时分交换系统的核心作用；

图 35 是说明 STM － n 单元的一种当前占用/备用的线路冗余方案的示意图；

图 36 是说明在一种含有插/分复用线路配置功能的环形应用中的传输设备的示意图。

现在将参照附图对本发明的优选实施方案加以描述。同样的参照数字用来表示在各个图中对应的或相等的组成部分。

图 1 是说明按照本发明的一种线路配置设备的功能框图。该线路配置设备的基本功能包括：

1)用于以基群信号（ Z － 1 ）的形式输入传输信号的功能；

2)信号同步；

3)用于交换时隙的 TSI（时隙交换）功能；

4)用于输出基群信号（ Z － 2 ）的功能；以及

5)用户接口功能。

一种为基群信号的中继信号，通过把低速信号复用成一种高速信号而形成。例如，具有由 IUT 所规定的 155.52Mbit/s 的传输速率的 STM－1 信号是通过复用具有作为 63 信道的等效值的 2.304Mbit/s 的传输速率的 TU－12 信号而形成的。

由 TSI 单元 3 所执行的 TSI 处理是为了改变经复用的低速信号的结构以获得一种高速信号，或者用另一种高速信号代替一种高速信号。根据本发明的交叉连接（线路配置）设备的性能之一提供了这样一种 TSI 功能。

图 1 所示方框的各个功能将进一步加以说明。首先，输入处理器 1 接收基群信号 Z－1，例如 STM－1 光信号，检测 ALM 数据，并且经过微机总线 S－9 把告警（ALM）数据信号 S－3 输出到信号同步器 2。在 ALM 出现的同时，输入处理器 1 把基群信号 Z－1 转换成 AIS 信号，并且以基群信号 S－1 的形式输出它。同样从输入处理器 1 输出的 S－2 信号是一种时钟信号。

信号同步器 2 从信号输入处理器 1 中获得基群 S－1 和 ALM 数据信号 S－3 的相位，并且把它们与那些相对于从 TSI 单元 3 得到的时钟信号 S－6 的相位进行交换，并以信号 S－4 和 S－5 的形式输出该结果。

信号同步器 2 在对称为 VC（虚容器）的各个线路信号的第一字节的位置定位的同时输出这些信号。一般来说，信号同步器 2 也用作弹性存贮器，并缓冲在信号输入处理器 1 和 TSI 单元 3 之间发生的频率变化。

TSI 单元 3 在每个时隙替换来自信号同步器 2 的基群信号 S－4，并且以 S－7 信号的形式按不同的序列顺序输出结果。在这时，根据 ALM 数据信号 S－5 并随着 ALM 的出现，信号 S－7 的内容发生改变。

在同一时刻，输出时钟 S－8，它与表示信号 S－7 的头部的定时脉冲的相位相同。

较出处理器 4 接收基群信号 S－7 以及时钟信号 S－8，并把它们转换成它输出的光信号 Z－2。来自用户接口 5 的开销数据经过总线接口 S－9 取出，并插入到基群信号 S－7 中。

现在将描述各个功能块的详细配置。

1) 输入处理器 1，用于以基群信号 Z－1 的形式输入传输信号:

为了处理一个所接收的基群信号 Z－1，必须确定该信号的头部位置。首先，完成基群信号 Z－1 的译码（例如解扰码）以确定基群信号 Z－1 的头部位置。

基群信号 Z－1 包括一种表示头部位置的特殊信号，如，一个固定的比特码型 A1 字节，为取得帧同步，将它插入到信号 STM－4 的开销部分中去。这种特殊的信号用于实现同步。

同步器 12 完成这种同步，并由一个具有一个帧周期的计数器和一个码型检测器组成。各种开销信号的位置以及存在于基群信号 Z－1 中的低速信号的位置可由计数器来指定。因此，提取各个低速信号的处理过程可按需要来实现。这种处理过程称为解复用（ DMUX ）。

经提取的各个开销数据被传送到开销数据处理器 13，开销数据处理器 13 对数据进行计算，如对 B1、 B2 和 B3 字节的完成计数。将检测到的 ALM 传递到 ALM 处理器 11。

ALM 处理器 11 收集由信号接收器 10 检测到的各种信号，并且按它们的优先次序进行处理，而且，例如，当没有检测到信号时， ALM 处理器 11 阻止信号的同步检测。

作为这些处理的结果， ALM 数据信号 a-6 和开销数据信号 a-7 由总线接口电路 14 传送到用户接口 5。

有时，由于 ALM 的出现，基群信号 Z－1 有必要经过处理以产生一种特殊的信号。当暂停光信号的接收时所进行的 AIS 处理就是一种处理实例。这种处理由信号转换器 15 来完成。在 AIS 处理中，根据 ALM 的出现，信号被屏蔽，并且设置为“1”。

图 2 是说明输入处理器 1 的功能框图。当接收的基群信号 Z－1 为光信号时，它必须转换成电信号。光/电信号转换器 10 完成光信号至电信号的转换，并且因此产生的电信号接着以信号 a-1 的形式输出。时钟信号 S-2 也被提取出来。

图 3 是说明所接收的基群信号 Z－1 为双极性信号的一种配置实例的示意图。在这种配置中，提供双极性信号转换器 10 取代光/电信号转换器 10。

双极性信号转换器 10 接收具有由 ITU 或 SONET 规定的双极性形式的电信号 Z－1－b，并且提取具有 NRZ 形式的数据单元 a-1 以及

来自电信号的时钟单元信号（ CLK ） S － 2 。

图 2 中的光/电信号转换器 10 接收具有由 ITU 或 SONET 规定的形式的光传输信号 Z － 1 ，并且提取具有 NRZ 形式的数据单元 a-1 以及来自光信号的时钟单元信号（ CLK ） S-2 。此外，转换器 10 检测 ALM 数据信号 a-3 ，例如，接收信号电平，它表示在接收信号中有异常，并且通知 ALM 处理器 11 。

类似地，在图 3 中，一种告警数据信号（ ALM ） a-3 传送到 ALM 检测器 11 ，这种告警数据信号表示输入的光信号或者输入的双极性信号具有预先确定的电平或更高的电平。

同步器 12 从光/电信号转换器 10 或双极性转换器 10 取出数据单元信号 a-1 ，并且提取复用在高次群中的低次群的信号 a-2 和 a-5 。信号 a-2 被传送到信号转换器 15 ，而开销数据信号 a-5 被传送到开销数据处理器 13 。

当数据信号接收时，数据信号 a-5 由开销处理器 13 进行处理，即，性能数据采用 B1 字节数据来计算。这些数据中， ALM 数据以信号 a-4 的形式输出，而其它数据以信号 a-7 的形式输出。在图 3 的配置中，ALM 数据信号 a-4 是直接从同步器 12 中传送的。

当信号 a-3 和 a-4 被接收时， ALM 处理器 11 完成它们的序列优先顺序处理，并输出用作信号转换器 15 的一种信号转换触发脉冲的控制信号 a-8 以及 ALM 数据信号 S － 8 。

响应于控制信号 S － 8 ，信号转换器 15 把从同步器 12 接收的基群信号 a-2 转换成另一种信号，例如 AIS 信号，这种信号又以信号 S － 1 的形式输出。

总线接口电路 14 从 ALM 处理器 11 以及开销数据处理器 13 中取出信号 a-6 和 a-7 ，并且把它们转换成总线数据信号 S － 9 ，然后输出。

2) 信号同步器 2

根据来自 TSI 单元 3 的时钟信号 S － 6 ，信号同步器 2 变换从输入处理器传送过来的基群信号 S － 1 和 ALM 数据信号 S － 3 的相位，并且以信号 S － 4 和 S － 5 的形式输出该结果。如图 4 所示，信号同步器 2 包括一个存贮器电路 20 、一个信号形式转换器 21 ，一个存贮器写入电路 22 以及一个存贮器读取电路 23 。

存贮器电路 20 ，这是一种用于以矩阵形式暂时存贮信号的设备，

它与来自存贮器写入电路 22 的写入时钟信号 b-1 同步，写入从输入处理器 1 接收的基群信号 S－1 以及 ALM 数据信号 S－3。

此外，根据来自存贮器读取电路 23 的读时钟信号 b-2，存贮器电路 20 也读取所有的存贮数据，或在 VC 部分中的数据信号（DATA）b-3 以及一种有关的 ALM 数据信号 b-4。

如果从存贮器电路 20 读取的数据信号（DATA）b-3 携带与信号 S－1 有关的所有内容，则信号 b-3 和 b-4 进行串并变换，以得到能易于由信号形式转换器 21 处理的形式。

当读出的数据（DATA）信号 b-3 是一种 VC 时，信号形式转换器 21 便在那里插入一种固定的填充信号或一种开销信号以对各个信道信号的头部位置进行定位，并以信号 S－4 的形式输出该结果信号。

对 ALM 数据信号 b-4 的定时进行调节以使得其相位与基群信号 s-4 的相位一致，并且经调节的 ALM 数据信号 b-4 以 ALM 信号 S－5 的形式输出

3) TSI 单元 3：

TSI 单元 3 的一种配置实例示于图 5。TSI 单元 3 包括一个 TSI 电路 30、一个控制信号发生器 31、一个总线接口电路 32 以及一个 UNEQUIPPED（未装备的）信号发生器 33。TSI 电路 30 在一个存贮器（图 5 未示出）中存贮所接收的基群信号 S－4，这个存贮器为 TSI 电路 30 的一部分。在来自控制信号发生器 31 的控制信号 C－1 的同时，控制信号以基群信号 S－7 的形式读出。

此时，TSI（时隙交换）是通过以一种与信号输入的顺序不同的序列顺序读取信号来完成的。

UNEQUIPPED（未装备的）信号发生器 30 产生并输出未装备信号，使得未装备信号也须经 TSI 处理。

为完成 TSI 处理，输入到 TSI 单元 3 的基群信号 S－4 的处于各级的头部位置被确定。首先，设置了在具有 150.336Mb/s 的比特率的虚容器 VC－4 的 J1 字节。

在图 6 中表示了具有同步相位的 STM－1 信号，该信号以 STM>1>AU-4>AUG-3>TUG-2>TU-12>TU-2 的形式进行映射变换。

在图 6 中*1 表示 STM－1 的开销的映射变换位置，第一字节被定义成 A1 字节。从而，TU－3 的指针字节和 TU－2/TU－12 的 V1 字

节处于第一行的位置，并且对所有体系等级的信号都整齐地排列。

为实现这种排列，把 VC－4 信号从 STM－1 信号中提取出来，并存入存贮器中。按预定的定时（按该预定的定时，可得到具有上述形式的映射）对这种信号进行重新映射。这一处理发生在信号同步器 2 中。

从信号同步器 2 的存贮器 20 中读出基群信号（VC－4 信号）与 TSI 单元 3 所需的预定的定时信号 S－6 相关。因此，映射以如图 6 所示的信号形式来实现。

这种处理示于图 7。STM－1 信号再一次存入 TSI 电路 30 的存贮器中以执行 TSI 处理。该 STM－1 信号预先变成并行信号以便于它写入至存贮器。

由于在 STM－1 信号中，一个字节是携带意义的最小信号单元，因此信号变成八个并行信号。这种处理由信号同步器 2 的存贮器读取电路 23 来完成。

为切换总线，根据字节数设置一种 ALM 信号。例如，对八个基群信号设置一种 ALM 信号。

TSI 单元 3 的 TSI 电路 30 一般如图 8 或图 9 至图 11 所示构成。采用图 8 所示的配置用于当收到输入信号 S－4 时对基群信号进行一般的处理。在图 9 至 11 中的配置用于把一种基群信号分开并且在几个存贮器中存贮分开的信号用于处理。

在图 8 中，TSI 电路 30 包括两个存贮器 300 和 301 以及一个信号选择器 302。基群信号 S－4 存贮在两个存贮器 300 和 301 中，并且根据来自信号选择器 302 的控制信号 C－1，以控制信号 S－7 的形式按与它写入的次序不同的顺序输出。

存贮器 300 和 301 有足够的存贮容量来存贮所有的基群信号以及在一个周期 T 期间接收的 ALM 数据，并且通过控制信号 C－1 进行访问。

传送到 TSI 单元 3 的基群信号 S－4 交替地写入存贮器 300 和 301。进行交替写入是为了能随机读取。数据必须在它全部都已存入存贮器 300 和 301 之后读取，使得存贮器 300 和 301 可作为相对于不断接收的基群信号不断地进行读和写的存贮器。

更具体地说，与控制信号 C－1 一致，TSI 电路 30 在 13.89ms 的周期内交替地取出基群信号 S－4 以及按一种改变的序列顺序读取基群信号 S－4，例如，如图 12 所示。根据控制信号 C－1，信号选择器

302 选择从已准备好读取的存贮器 300 和 301 中读取的信号 C1 - 1.1 和 C1 - 1.2 中的一种，并且以基群信号 S - 7 的形式输出该选择的信号。

当按照信号 C - 1 指定的未装备（ UNEQUIPPED ）信号的选择时，就选出一种未装备信号 C - 4 。

图 9 所示的 TSI 电路 30 的另一种配置包括 2n 存贮器组 300 - 1 至 n 和 301 - 1 至 n， n 个信号选择器 302 - 1 至 n，以及一个信号选择器 303 。

在图 10 所示的另一种配置中， TSI 电路 30 对每一种基群信号 S - 4.1 至 S - 4.n 都具有图 8 中的结构。此外，还设置了一个第二信号选择器 303 以及一个并/串变换器 304 。

对于图 11 所示的配置，设置了一个第三信号选择器 305 以选择基群信号。

在图 11 对 TSI 电路 30 的配置中，除了在图 9 对 TSI 电路 30 的配置之外，还在信号选择器 303 的后级设置了串/并变换电路 304，并在串/并变换电路 304 之后设置了信号选择器 305 以根据控制信号 C2 - 7 切换通道。信号选择器 305 分析所所接收的信号以得到几种基群信号 S - 7.1 至 S - 7.m，然后输出。

由于在图 9 至图 11 中对 TSI 电路的配置，从而基群信号存贮在若干存贮器中，当存贮在控制信号发生器 31 内的存贮器 313 中的读地址数据的数量增加时，读控制信号 C - 1 的速率相应地增大，相对于 TSI 电路 30 的基群信号 S - 7 的数量也增加。

在图 9 至图 11 中，各个存贮器组 300 - 1 至 300 - n 和 301 - 1 至 301 - n 的结构与在图 8 中的存贮器 300 和 301 的结构相同。这些存贮器有足够的存贮容量以存贮所有的基群信号 S - 4.n(n=1 至 n)和在周期 T 期间接收的 ALM 数据，并且可根据控制信号 C - 1n 进行访问。

取出基群信号 S - 4.0n （ n=1 至 n ）。并且根据控制信号 C - 1.n （ C - 1 包括如下面将描述的来自控制信号发生器的 CLK 信号 C - 1 CLK，和 ACM 数据信号 C - 1.acm1, C - 1.acm2 以及 C - 1.sel ），按照不同于所接收的信号的序列顺序，交替地读出基群信号 C1 - 1.1.1 至 C1 - 1.1.n 和 C1 - 1.2.1 至 C1 - 1.2.n 。

当控制信号 C - 1 指定选择未装备（ UNEQUIPPED ）信号时，选择一种未装备信号。

信号选择器 302 - 1 至 302 - n 从存贮器组 300 - 1 至 300 - n 和 301 - 1 至 301 - n 中接收基群信号 C1 - 1.1.1 至 C1 - 1.1.n 和 C1 - 1.2.1 至 C1 - 1.2.n，并且按照来自控制信号发生器 31（见图 5）的控制信号 C - 1.sel 选择读取就绪的信号。

根据以下将描述的从控制信号发生器 31 接收的控制信号 C - 1.sel2，信号选择器 303 从来自信号选择器 302 - 1 至 302-n 的基群信号 C1 - 2.1 至 C1 - 2.n 中选择一种信号，选出的信号以基群信号 S - 7 的形式输出。

TSI 单元 3 的控制信号发生器 31 输出与时隙交换（信号交换）有关的主时钟信号 S - 6.CLK， S - 1.CLK、和 S - 8.CLK 以及用于控制 TSI 电路 30 的控制信号 C - 1（ C - 1.sel, C-1.acm1 和 C-1.acm2 ）。

例如，控制信号发生器 31 含有如图 13 所示的配置，并且与图 8 中的 TSI 电路 30 合起来使用。这种控制信号发生器 31 没有通道交换功能，它包括一个时钟（ CLK ）振荡器 310 、一个脉冲发生器 311 、一个控制选择器 312 、一个存贮器 313 以及一个存贮控制器 314 。

时钟（ CLK ）振荡器 310 产生与时隙交换（信号交换）有关的主时钟信号 S - 6.CLK 、 C - 1.CLK 和 C2 - 1 。脉冲发生器 311 产生 TSI 处理所需的各种定时脉冲信号 S - 6.tp 和 S - 8.tp，以及针对 TSI 电路 30 的控制信号 C - 1.sel 。

数据信号 C2 - 4，为 TSI 电路 30 的存贮器 300 和 301 的读地址信号，它通过存贮控制器 314 传送到并存于存贮器 313 中。这种信号根据来自脉冲发生器 311 的控制信号 C2 - 2，以控制信号 C2 - 6 的形式周期性地输出。

存贮控制器 314 从总线接口电路 32 取出 TSI 设置（ setting ）数据信号 C - 3（见图 5），并将它写入存贮器 313 。存贮控制器 314 也输出数据信号 C2 - 4 至总线接口电路 32，作为设置信号的确认，并且为了确认，从存贮器 313 中读取地址数据。

控制信号选择器 312 选择来自脉冲发生器 311 的写地址信号 C2 - 2 或者来自存贮器 313 的读地址信号 C2 - 6 。

写地址信号 C2 - 2 是一种递增计数信号，它是一种顺序地写入存贮器 313 的地址信号。在与针对存贮器 313 的重复读取和写入同步中，写地址信号 C2 - 2 和 TSI 控制信号 C2 - 6 由控制信号选择器 312 交

替地加以选择，并且以控制信号 C－1.acm1 和 C－1.acm2 的形式输出。

读/写存贮器 313 的周期是一行所需的时间周期（125/9ms）。由于 STM－1 信号对每一行有相同的信号排列，如图 6 所示，只需取出一行数据就足以完成 TSI（时隙交换）。

当信号格式受到限制时，甚至 1/4 行数据也可使 TSI 处理实现。一旦数据已经存于存贮器中，它们可以在输出时随意读取。这种特性用于实现 TSI 功能。如图 14 所示，通过对存贮器输入时刻与存贮器输出时刻进行比较，行 100 和 101 得以交换。

当设置了许多存贮器 313 时，它们可由一个选择器来加以选择。同样，有一种根据 ALM 数据选择存贮器控制信号的方法以及一种用于在 TSI 之后选择基群信号的方法适用于交换通道。

根据用于选择存贮控制信号的方法，当 ALM 出现时将所选择的信号的数据预先存贮在存贮器 313－1 和 313－2 中，如在图 15 的控制信号发生器 31 的一种配置实例中所示。

此外，设置了一个信号鉴别器 316 和一个第二控制信号选择器 315，以根据 ALM 出现期间的情况选择存贮器 313－1 和 313－2 的一种输出。由于根据 ALM 出现期间的情况控制信号发生改变，基群信号相应地发生改变。

在图 5 中控制信号发生器 31 的实例对应于图 8 中的 TSI 电路 30，但含有通道交换功能。控制信号发生器 31 包括一个时钟振荡器 310、一个脉冲发生器 311、一个控制信号选择器 312、存贮器 313－1 和 313－2，一个存贮控制器 314 以及一个信号鉴别器 316。

控制信号发生器 31 产生与交叉连接（信号交换）有关的主时钟信号（CLKS）S－6.CLK、C－1.CLK 和 S-8.CLK。此外，控制信号发生器 31 输出用于控制码组定时的定时脉冲信号 S－6.tp 和 S－8.tp，以及用于控制 TSI 电路 30 的控制信号 C－1（C－1.sel，C－1.acm1 和 C-1.acm2）。

这种配置与在图 13 中对控制信号发生器 31 的配置之间的区别是接收了一种 ALM 数据信号 S－5，并且据此，用于控制 TSI 电路 30 的存贮器 300 和 301 的控制信号 C－1.acm1 和 C-1.acm2 的内容发生了改变。

而且，在图 15 中，除了对于在图 8 中 TSI 电路 30 的配置外，作为存贮器 300 和 301 的读地址信号的数据信号 C - 2.4.1 和 C2 - 4.2 通过存贮控制器 314 传送到并存于存贮器 313 - 1 和 313 - 2 中。这些信号根据来自脉冲发生器 311 的控制信号周期性地输出。

在图 15 中，随着与 TSI 电路 30 中的存贮器相对应的存贮器数量增加，从存贮控制器 314 的信号输出增至 C2 - 4.1 和 C2 - 4.2，而输入信号增至 C2 - 5.1 和 C2 - 5.12。

信号鉴别器 316 根据来自信号同步器 2 的线路 ALM 信号 S - 5，输出用于选择存贮器 313 - 1 和 313 - 2 之一的选择信号。控制信号选择器 312 根据来自信号鉴别器 316 的控制信号 C2 - 7 选择从存贮器 313 - 1 和 313 - 2 输出的读地址信号中的一个。

根据图 15 中的配置，控制信号选择器 312 选择从脉冲发生器 311 输出的写地址信号 C2 - 2 以及从选择器 315 输出的信号 C2 - 6.C。

在图 16 中示出了对应于图 9 的控制信号发生器 31。该控制信号发生器 31 没有通道交换功能，并且包括一个 CLK 控制器 310、一个脉冲发生器 311、一个控制信号选择器 312、一个存贮器 313 以及一个存贮控制器 314。

图 16 中的控制信号发生器 31 产生与时隙交换（信号交换）有关的主时钟信号（ CLKS ） S - 6.CLK， C - 1.CLK 和 S - 8.CLK。控制信号发生器 31 也输出用于控制码组的定时的定时脉冲信号 S - 6.tp 和 S - 8.tp，以及用于控制 TSI 电路 30 的控制信号 C - 1（ C - 1.sel、C - 1.acm1、 C - 1.acm2 和 C - 1.sel2 ）。

数据信号 C2 - 4 用作存贮器 300 和 301 的读地址信号，它通过存贮控制器 314 传送并存于存贮器 313 中，并且根据来自脉冲发生器 311 的控制信号 C2 - 2，以控制信号 C2 - 6 的形式周期性地输出。当这种信号由图 9 中的 TSI 电路 30 采用时，用于控制 TSI 电路 30 的信号选择器 303 的信号 C - 1.sel2 也得以输出。

含有图 17 中的配置的控制信号发生器 31 对应于图 9 中的 TSI 电路 30，但含有通路交换功能。图 17 中的控制信号发生器 31 包括一个 CLK 振荡器 310、一个脉冲发生器 311、一个控制信号选择器 316、存贮器 31301 和 313 - 2，一个存贮控制器 314、一个信号鉴别器 315 以及一个控制信号选择器 312。

图 17 中的控制信号发生器 31 产生为与信号交换有关的主时钟的时钟信号（ CLKS ） S － 6.CLK 、 C － 1.CLK 和 S － 8.CLK ，也输出用于控制码组的定时的定时脉冲信号 S － 6.tp 和 S-8.tp .

控制信号发生器 31 同样输出用于控制 TSI 电路 30 的控制信号 C － 1（ C － 1.sel 、 C-1.acm1 、 C － 1.acm2 和 C-1.sel2 ）。

这种发生器与图 16 中的控制信号发生器 31 之间的区别是接收一种 ALM 数据信号 S － 5，并且根据该数据，使用于控制 TSI 电路 30 的存贮器 300 和 301 的控制信号 C － 1.acm1 、 C － 1.acm2 和 C － 1.sel2 的内容发生了改变。

在图 18 中示出了对应于图 11 中的 TSI 电路 30 的控制信号发生器的一种实例。除了图 16 所示的配置外，设置了信号鉴别器 315 ，以接收 ALM 数据信号 S － 5 以及输出控制信号 C2 － 7 。

4) 传输信号发生器 4：

图 19 是说明传输信号发生器 4 （见图 1 ）的一种配置实例的示意图。传输信号发生器 4 包括一个存贮电路 40 、一个存贮器读取电路 41 、一个开销字节插入电路 42 、一个信号复用器 43 、一个信号转换器 44 以及一个总线接口电路 45 。

传输信号发生器 4 接收来自 TSI 单元 3 的基群信号 S － 7 、时钟信号 S － 8.CLK 和定时脉冲信号 S － 8.tp，并把它们转换成光信号 Z － 2，然后输出。

此时，传输信号发生器 4 经过总线接口 S － 9 从用户接口单元 5 中取出开销数据，并且将它插入到基群信号 S － 7 中。

存贮电路 40 取出并存贮通过 TSI 单元 3 输入的基群信号 S － 7 。此外，根据来自存贮器读取电路 41 的读时钟信号 d-1 ，存贮电路 40 输出所存贮的数据。

存贮器读取电路 41 接收来自 TSI 单元 3 的时钟信号 S － 8.CLK 和定时脉冲信号 S － 8.tp ，并且输出用于控制存贮电路 40 的读取的读时钟信号 d-1 。

开销字节插入电路 42 取出从存贮电路 40 读取的基群信号 d-2 ，并把开销数据插入到预定的时隙中。在这个时候，开销字节插入电路 42 也从总线接口电路中取出开销数据 d-3 ，并且把它插入到预定的时隙中。

信号复用器 43 完成从开销字节插入电路 42 接收的基群信号 d-4 的串/并变换，以得到一种适合于信号转换器 44 的信号形式。在这时，信号复用器 43 同样进行一种编码处理，如扰码。

信号转换器 44 含有电/光信号转换功能，它把来自信号复用器 43 的基群信号 d-5 转换成光信号 Z－2，如 STM－1 信号，然后输出。

总线接口电路 45 通过用于传输由用户为开销字节插入电路 42 指定的开销数据信号 d-3 的总线连到用户接口单元 5。

不作为电/光信号转换器，信号转换器 44 可以是一种输出双极性信号的输出电路，这种双极性信号是一种电信号。

起双极性信号的输出电路作用的信号转换器 44，以一种如 140Mbps 的电信号形式输出来自信号复用器 43 的信号。

由 TSI 单元 3 输出的基群信号传送到信号发生器中的存贮器 40。这种情况的出现是由于基群信号变成一种时钟信号源，这种时钟信号源不同于 TSI 单元 3 的 CLK 振荡器 310 的时钟信号源，但是与 CLK 振荡器 310 同步。

此时，AU－4 指针被替换。此外，开销数据由开销字节插入电路 42 插入到基群信号中的一个特殊位置。同样插入的是用于客户建立的数据，这种数据是从连到用户接口单元 5 的总线接口电路 45 接收的。

接下来，对基群信号进行串/并变换以得到一种适合于信号转换器 44 的信号形式。在这个时候，同样进行基群信号的编码（扰码），奇偶校验的屏蔽，以及 B1 字节的插入等。

最后，该结果信号通过信号转换器 44 转换成光信号 Z－2，并且输出该光信号 Z－2。

5) 用户接口功能

用户接口单元 5 的功能是对于所接收的基群信号的 ALM 数据的处理、在一个显示器或一个终端上性能数据和开销数据的显示、通过一个计算电路对客户建立的线路数据的计算、通过使用一种总线信号把结果传输到 TSI 单元 3、以及把用于客户建立的开销数据传输到信号发生器 4。

更具体地说，用户接口单元 5 完成一种中间处理，用于把由用户完成的设置经过总线 S－9 传送到信号接收器 1、TSI 单元 3 或信号发生器 4，或者用于显示收到的基群信号的状态（ALM，等）和包括在那

个信号中的开销数据。

用户接口单元 5 的一种实例示于图 20。用户接口单元 5 包括一个总线控制器 50、一个存贮器 51、一个 CPU52 以及一个外部接口电路 53。

总线控制器 50 经过总线 S－9 连到信号输入处理器 1、TSI 单元 3 或者信号发生器 4 的总线接口电路，用于 ALM 数据和开销数据的交换。

在存贮器 51 中存有由用户指定的线路配置数据、通过开销或输入信号处理器 1 收集的 ALM 数据、以及由 CPU52 采用的用于计算的暂时数据。

CPU52 连到总线控制器 50、存贮器 51 以及外部接口电路 53，并且通过进行计算改变输入/输出数据的格式。

外部接口电路 53 含有用于各种设备如显示设备、键盘以及便携终端的接口端口以提供接口给用户。外部接口电路 53 从这些设备把数据传送到 CPU52，并且经由 CPU52 从接口端口输出存贮在存贮器 51 中的各种数据。

图 21 是说明以上详细描述的本发明用于完成当输入 STM－4×2 线和 STM－1×8 线时的交叉连接（线路配置）的一种实施方案的示意图。

在图 21 中，用于以上描述的示意图经部分简化，并且使连接的顺序发生了改变。如图 21 所示，两个 STM－4 信号以及八个 STM－1 信号输入到信号输入处理器 1，并且由信号输入处理器 1 中的光/电信号转换器 10 转换成电信号。

STM－1 信号复用在 STM－4 信号中，并且信号输入处理器 1 中的 ALM 处理器 11 通过使用 STM－1 等级信号共同处理 ALM 监控信号。因此，STM－4 信号由信号输入处理器 1 的同步器 12 分成四个 STM－1 信号。

由于输入到交叉连接（线路配置）设备的 STM-n 信号各有不同的帧定时，它们的时隙位置必须定位以进行交叉连接。

因此，与示于图 4 的信号同步器 2 的存贮器 20 有关的写和读定时受到控制，并且所有的输入 STM－1 信号的帧定时位置受到调节，使得它们彼此一致。

处理 ALM 监控信号的 ALM 处理器 11 对复用到各输入 STM－1

信号中的 VC-n 信号的 ALM（告警）状态的各信道进行监控。

按照监控的 ALM 状态，输出一种表示各信道状态的信号： SF（信号失败）、 SD（信号恶化）、或 NO - ALM。

然后，当基群信号数据以及告警信号的接收时，信号同步器 2 的信号转换器 21 复用 STM - 1 信号，以得到一种 STM - 4 信号，以使线路配置更为方便。该合成的信号 STM - 4 被传送到 TSI 单元 3。

在 TSI 单元 3 中的未装备（ UNEQ ）信号发生器产生一种由等效的 252 个信道复用 VC - 12 未装备（ UNEQUIPPED)信号得到的 STM - 4 信号。在 TSI 单元 3 中的 TSI 电路 30 包括线路配置电路 131 至 164。

当把图 21 的实施例中的 TSI 电路 30 与前面所描述的 TSI 电路实例 30 比较时，这对应于图 22A 和 22B 具体所示的比较。也就是说，在图 22A 中的结构对应于以前所描述的 TSI 电路 30 的配置，其中线路配置单元 100 对应于存贮器 300 和 301 以及信号选择器 302 组成的装配单元。选择器 101 对应于选择器 303（见图 9）。

线路配置单元 100 的输出共同传送到选择器 101，选择器 101 选择这些输出的一种。

另一方面，在图 21 所示的实施例中，如图 22B 所示，每一种线路配置单元 131 至 164 是级联的，这种线路配置单元各由一个线路配置单元 100 和一个选择器 102 组成。

在图 21 的实施例中，设置了总共 16 个线路配置单元，因为每一套垂直设置的四个单元完成一个 STM - 4 的 TSI(共四套对应于一个 STM - 16)。由于设备的速率是有限的，一套垂直的单元不能完成一个 STM - 16 的 TSI。因此，速率降至 1/4，而线路规模的大小增加四倍。

由 TSI 电路处理的数据量可根据寻址速率发生变化。如果设置寻址速率等于一个 STM - 16，图 21 的一套线路配置单元就足够了。

在图 21 的实施例中，从信号转换器 21 接收的 STM - 4 信号的一种任选 VC - n 信号插入到从未装备（ UNEQ ）信号发生器 33 或较高级线路配置电路传送的直通信号中。此时，对加到 VC - n 的一种状态信号也进行线路配置。

此外，设置线路选择器（通道交换： PW ） 140 和 141 以按照加到 VC - n 的状态信号选择由线路配置电路 131 至 164 交叉连接的信号中的一个。

对于没有进行冗余处理的信道，信号在没有作出选择的情况下输出。就这种配置来说，由于线路配置单元的连接按多级垂直增加，输入信号的容量也就增加了。如果线路配置单元的连接按多级水平增加，就增加了输出信号的容量。因此，总的来说，线路配置容量可以容易地增加。

在图 21 的实施例中每一种线路配置电路 131 至 164 的一种配置实例示于图 23 。线路配置单元 100 包括一个数据存贮器。数据存贮器 100 有两面（ sides ），每一面含有足够的存贮容量以存贮一行 STM － 4 信号（ 125/9μs ）以及一个三比特的 ALM 信号。

由于信道的重复是对每一行进行的，所以每一面含有一行的存贮容量。在信号按输入次序从左开始写在一面的同时，将最接近的前一行数据写在另一面，并且根据来自地址存贮器 103 的地址读出任选数据。按这种方式，对于每一行，写和读都发生改变。

在要输出的信号的一行中，每个数据字节的输入源数据存贮在地址存贮器 103 中。以下的输入源数据存贮在存贮器中，并且可以由外部重写：

（ 1 ）不管数据是来自一种直通输入，还是读自数据存贮器 100；以及

（ 2 ）将要从数据存贮器 100 读取的数据的地址。

数据存贮器的输出和直通数据传递到选择器 102 。按照地址存贮器 103 的内容，选出直通数据或者来自数据存贮器 100 的数据。在这种选择之前，两种数据的帧定时位置应该一致。

对于图 21 中的实施例中的各个信号的时序图示于图 24 和 25 。在图 24 的括弧中的参照数对应于图 21 的参照数。

图 26 是另一实施例的示意图，它是按照 ALM 数据选择存贮器控制信号的一种通道交换实例。象图 21 一样，也使用 STM － 4 × 2 和 STM －1 × 8 作为输入，以进行交叉连接。

如同在图 21 的实施例中，经复用的 STM － 4 信号的独立 VC － n 插入到从未装备（ UNEQ ）发生器或从线路配置电路发送的直通信号中。在这个时候，对于加到 VC － n 的状态信号也进行线路配置。

在一设定时隙上，对来自较高级的信号的 ALM 及要插入的信号的 ALM 进行监控，并且对具有较好质量的信号进行选择。因此，可提供

冗余功能。

图 27 是说明用于图 26 中的实施例的线路配置电路的配置的示意图。这种电路和用于图 21 所示实施例的图 23 中的线路配置电路之间的区别是设置了一个选择鉴别器 104。选择鉴别器 104 对应于控制信号选择器 312 和鉴别器 315（例如，见图 17），这两者在前面都描述过。

数据存贮器 100 有两个存贮面，每一面含有足够的容量以存贮一行（125/9μs）STM－4 信号以及一个三比特的 ALM 信号。

由于信道的重复是对每一行进行的，所以每一面含有足以满足一行的存贮容量。在信号按序列输入次序从左开始写在一面的同时，最接近的前一行数据写在另一面，并且根据来自地址存贮器 103 的地址读出任选数据。按这种方式，对于每一行写和读都发生变换。

在要输出的信号的一行中的每一数据字节的输入源数据以及用于确定是否应该进行冗余处理的数据，存贮在地址存贮器 103 中。在存贮器中的数据可由外部重写。以下输入源数据被存贮：

（1）不管数据是来自一种直通输入，还是读自数据存贮器；

（2）将要从数据存贮器 100 读取的数据的地址；以及

（3）用于该数据的时隙是否应该是冗余的。

选择鉴别器 104 使用来自地址存贮器 103 的数据（1）和（3）以及来自信号的 ALM 数据，以确定应当选择直通数据还是来自数据存贮器 100 的数据。确定的内容示于图 28。

根据选择鉴别器 104 作出的确定结果，选择器 102 根据地址存贮器 103 的内容选择直通数据或者来自数据存贮器 100 的数据。为了选择，两种数据的帧定时位置必须一致。

在图 26 的实施例中各个信号的时序图示于图 29 和 30。在图 29 的括弧中的参照数对应于图 26 中的参照数。

通过使用图 23 的线路配置电路，可以如图 31 所示配置一种插/分复用器（MUX）。插/分复用器是一种多路复用器，通过它，相对于双向高次群信号，使单向低次群信号相互接口，而且对于这种复用器，交叉连接功能受到限制。

由于这种限制，对于高次信号群之间的连接的时隙交换受到禁止。对于高次和低次群之间的连接，时隙可自由地交换。在图 31 的这种实施例中的各个信号的时序图示于图 32 和 33。在图 32 的括弧中的参照

数对应于图 31 的参照数。

如在以上所述的实例方案中，根据本发明，可以提供大规模的线路配置功能。由于获得了线路配置的高可靠性，可以得到线路冗余功能以及一种有效的电路结构。因此，能提供一种电路结构，在这种电路结构中，线路配置功能的有效和无效的设置是灵活而有效的。

此外，通过使用相同的线路配置电路，可以配置一种插/分复用器。

以上说明的实施方案以及附图仅用于说明本发明，因此，本发明并不只限于这些实施方案和附图。本发明保护的范围由所附的权利要求书的描述来确定，并且与权利要求书等效的内容都在本发明的范围之内。

说 明 书 附 图

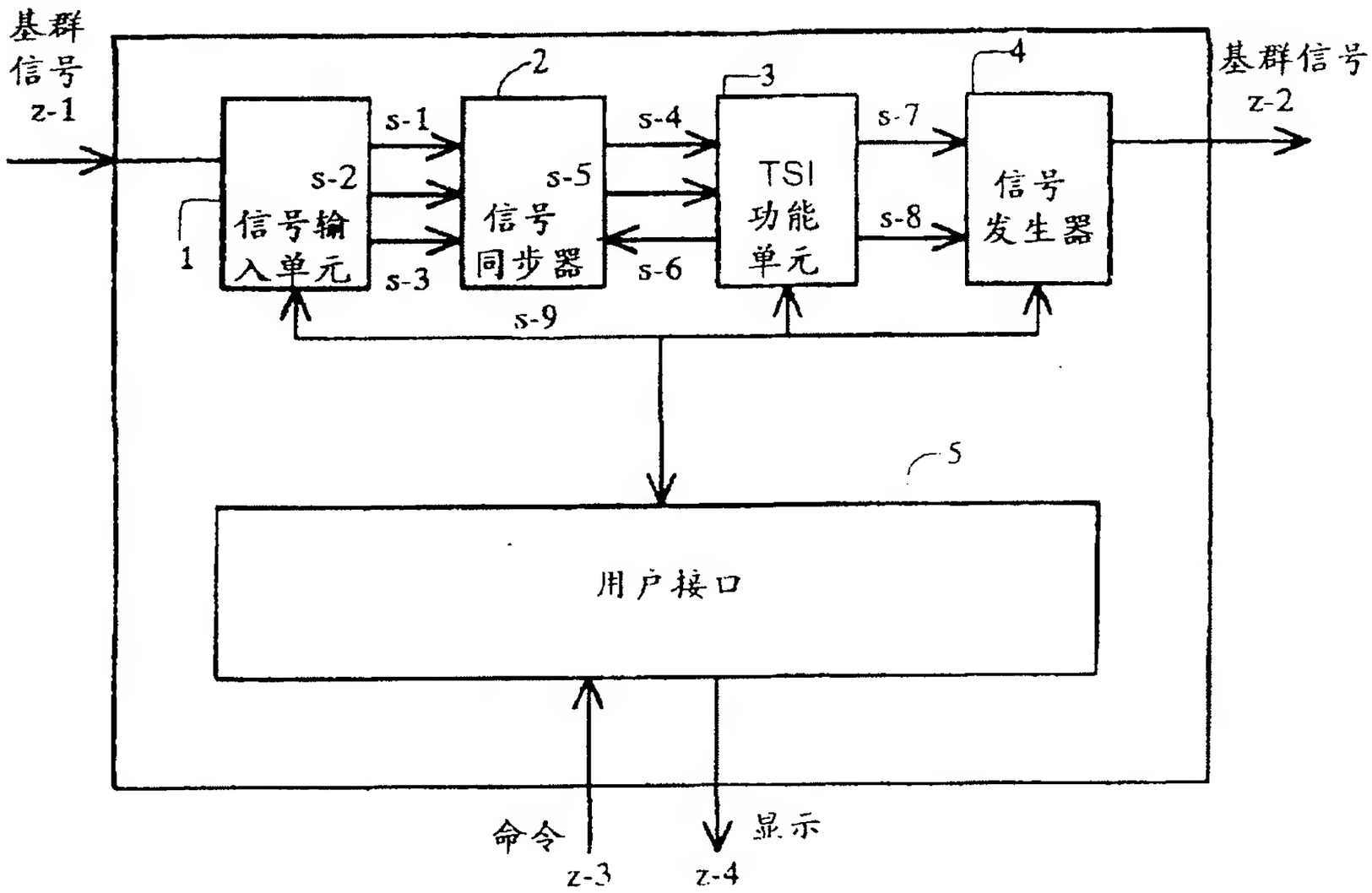

基群
信号
z-1
1
s-1
s-2
s-3
信号输
入单元
2
s-5
信号
同步器
s-4
s-6
3
TSI
功能
单元
s-7
s-8
4
信号
发生器
基群信号
z-2
s-9
5
用户接口
命令
z-3
显示
z-4

图 1

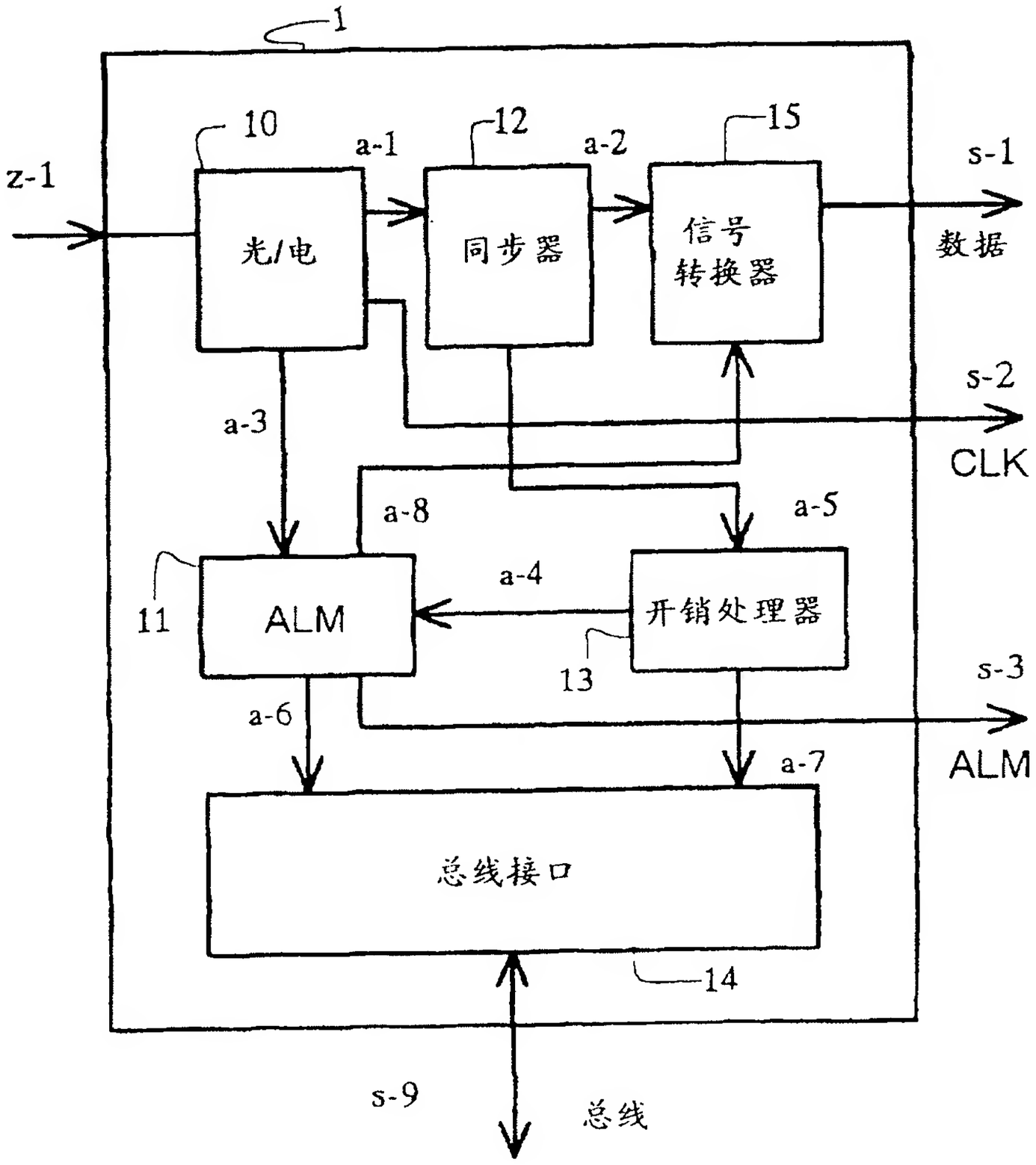

1
10
12
15
z-1
a-1
a-2
s-1
光/电
同步器
信号
转换器
数据
s-2
a-3
CLK
a-8
a-5
11
ALM
a-4
开销处理器
13
s-3
a-6
ALM
a-7
总线接口
14
s-9
总线

图 2

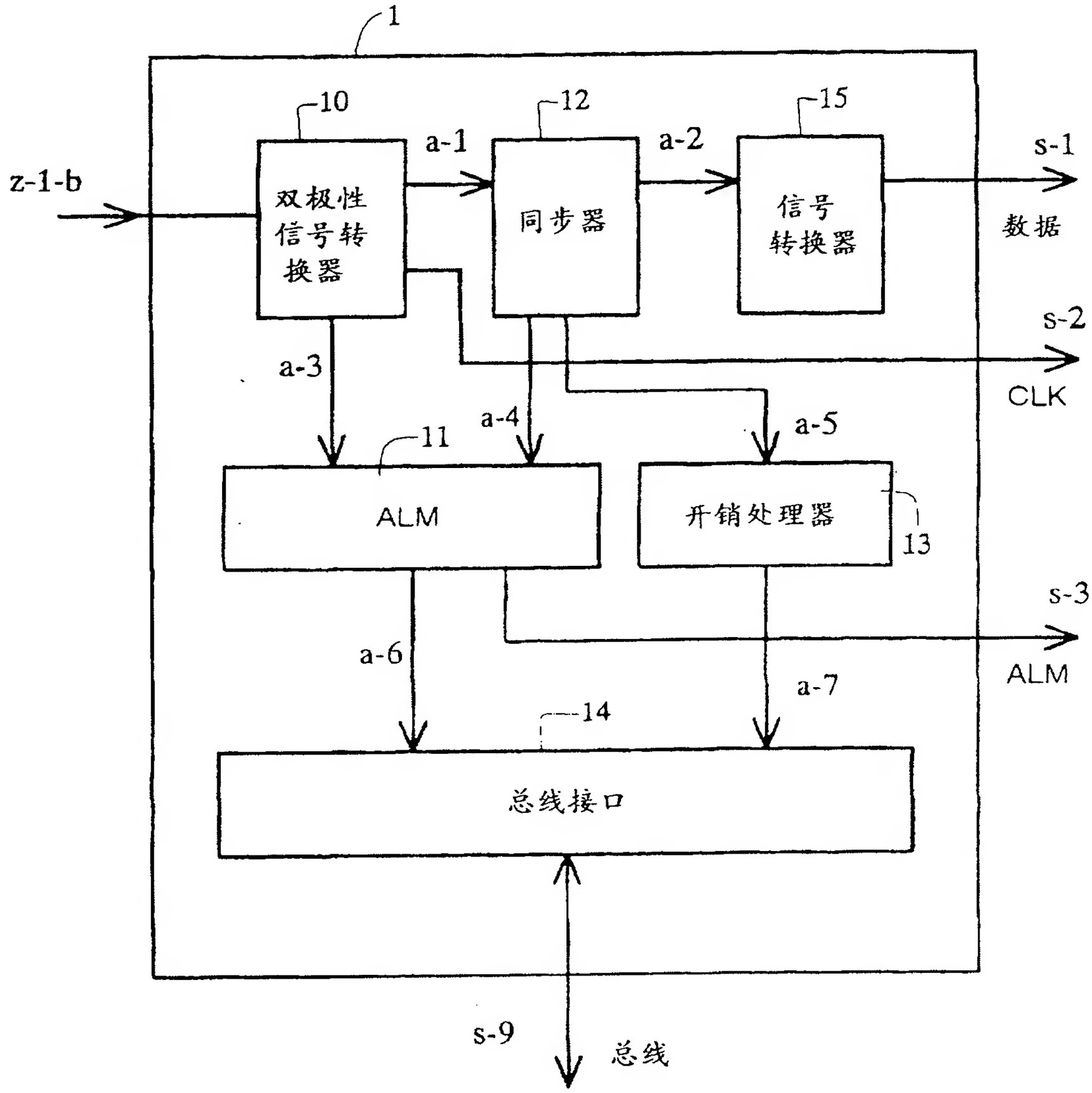

1
10
12
15
a-1
a-2
s-1
z-1-b
双极性信号转换器
同步器
信号转换器
数据
s-2
a-3
CLK
a-4
a-5
11
ALM
开销处理器
13
s-3
a-6
ALM
a-7
14
总线接口
s-9
总线

图 3

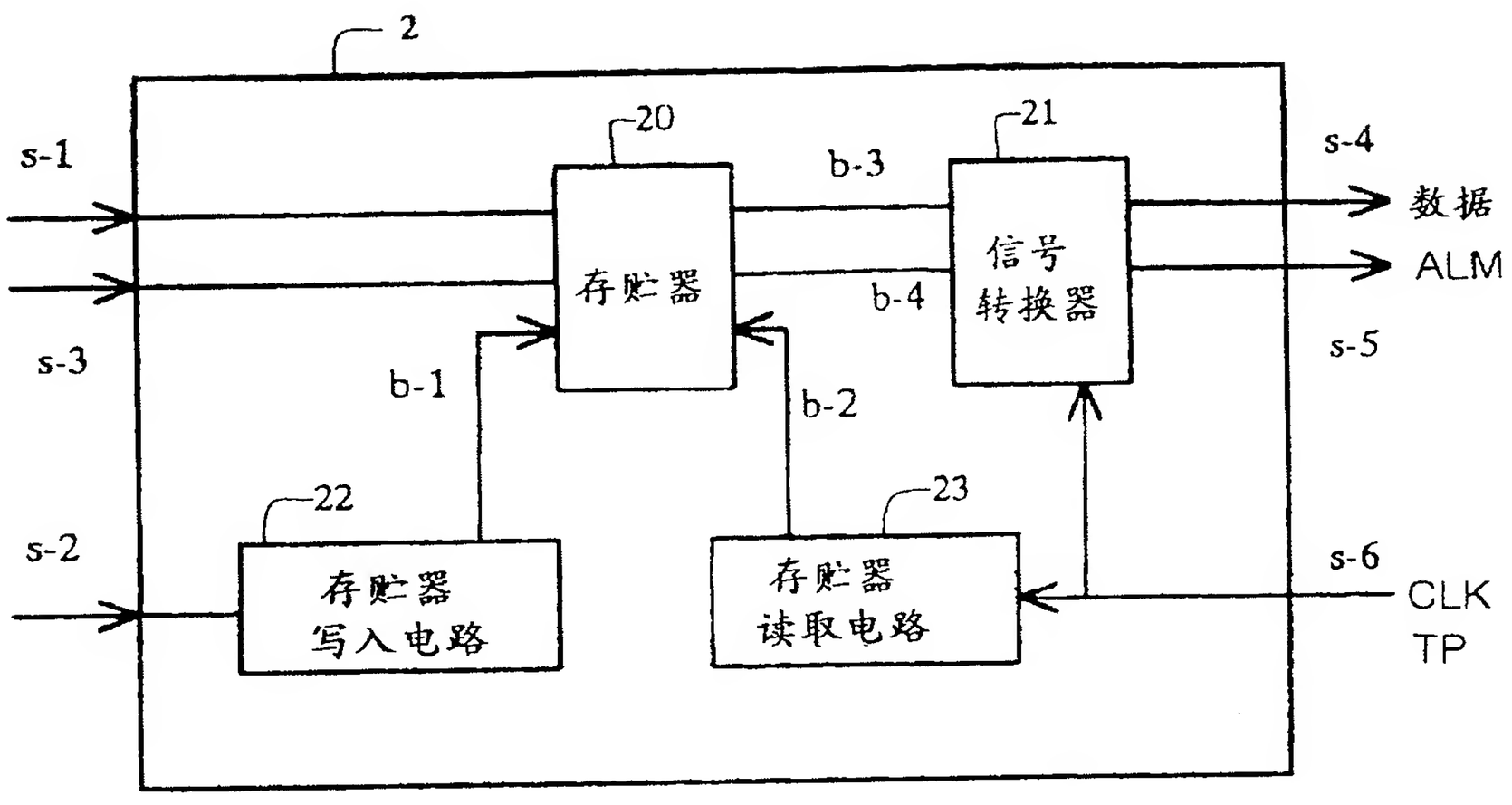

2
20
21
s-1
b-3
s-4
数据
存贮器
信号
转换器
ALM
b-4
s-3
s-5
b-1
b-2
22
23
s-2
s-6
存贮器
写入电路
存贮器
读取电路
CLK
TP

图 4

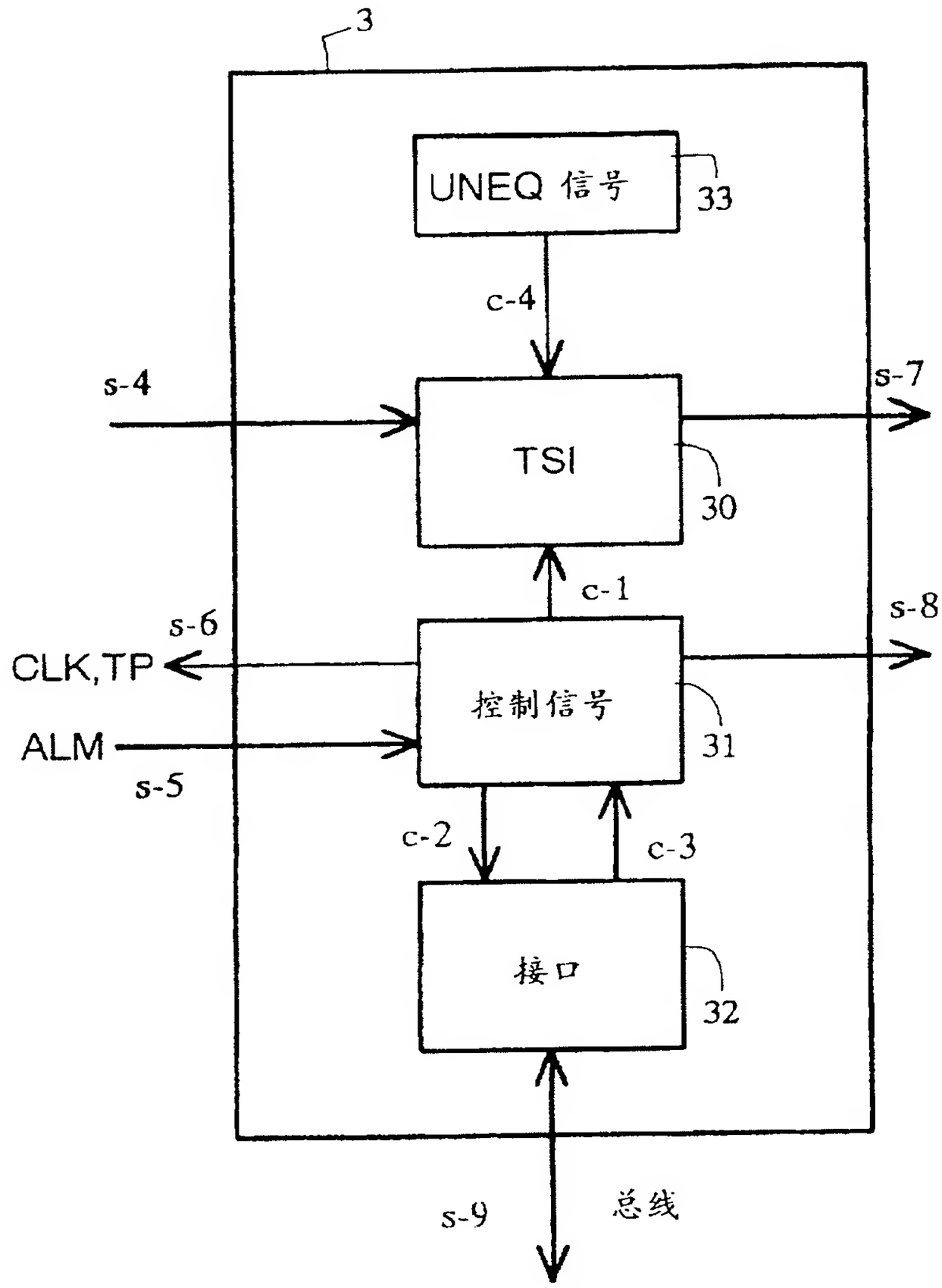

3
UNEQ 信号
33
c-4
s-4
TSI
30
s-7
c-1
s-6
CLK,TP
控制信号
31
s-8
ALM
s-5
c-2
c-3
接口
32
s-9
总线

图 5

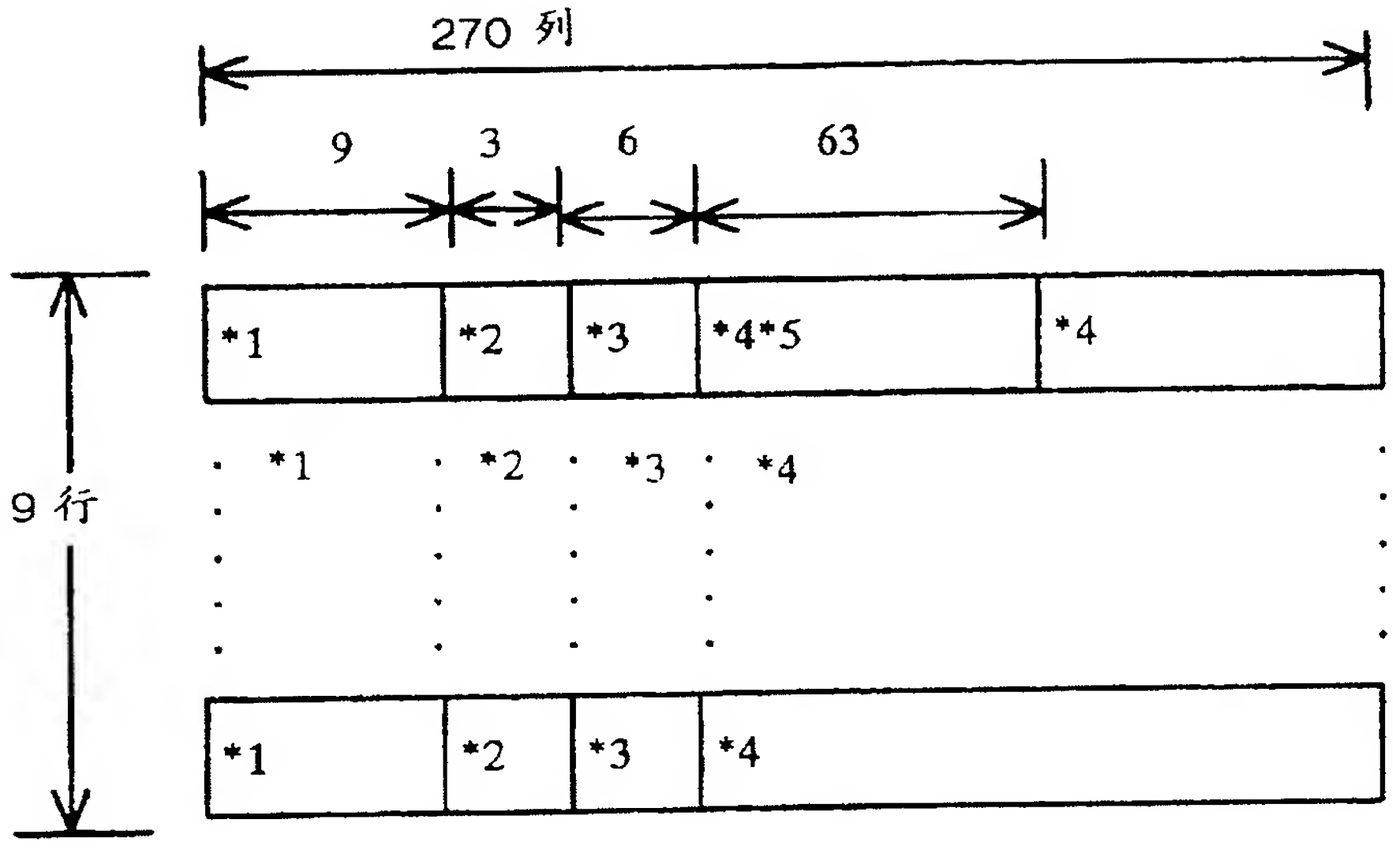
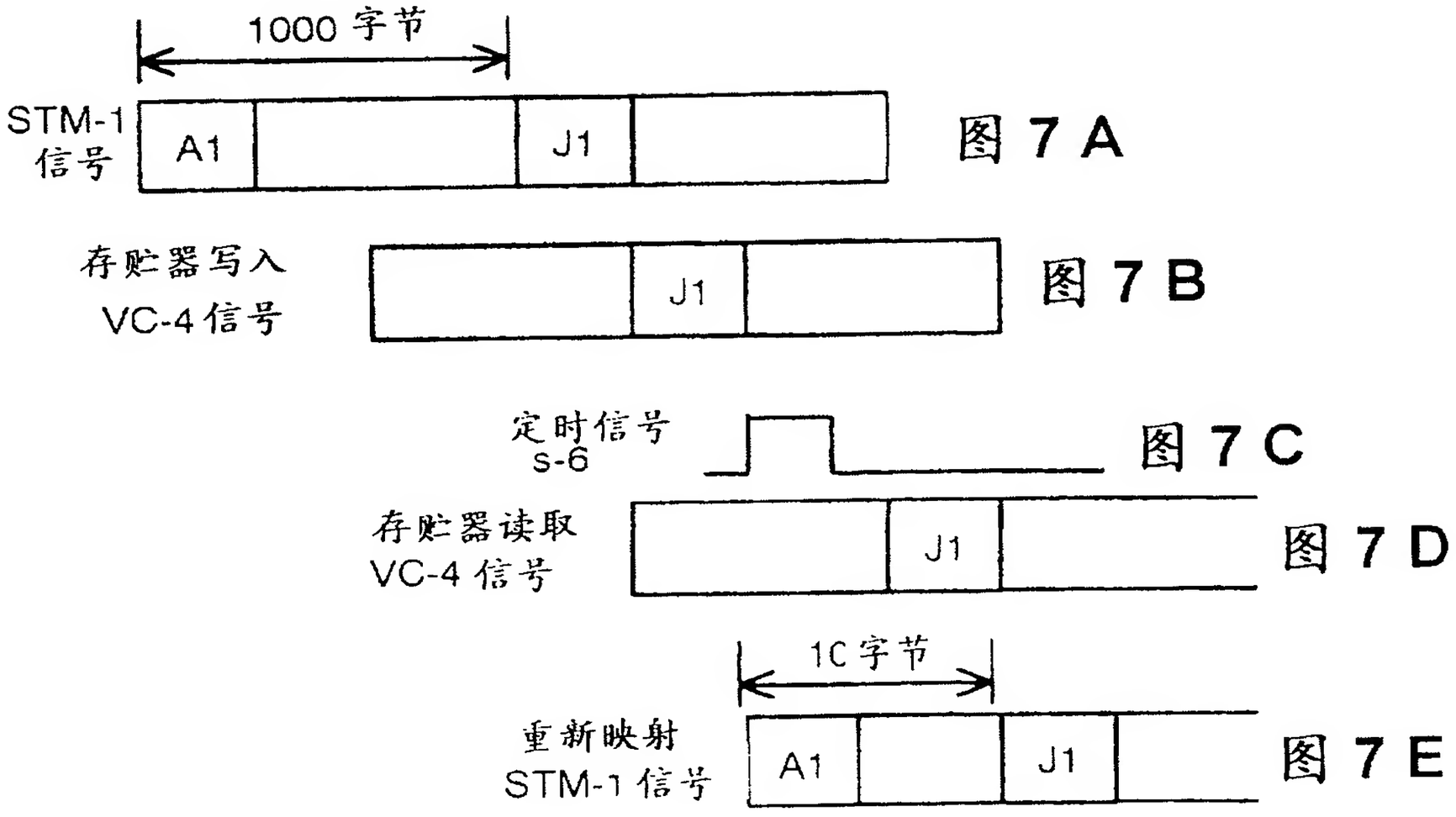


图 6


1000 字节
STM-1
信号
A1
J1
图 7 A
存贮器写入
VC-4 信号
J1
图 7 B
定时信号
s-6
图 7 C
存贮器读取
VC-4 信号
J1
图 7 D
1C 字节
重新映射
STM-1 信号
A1
J1
图 7 E

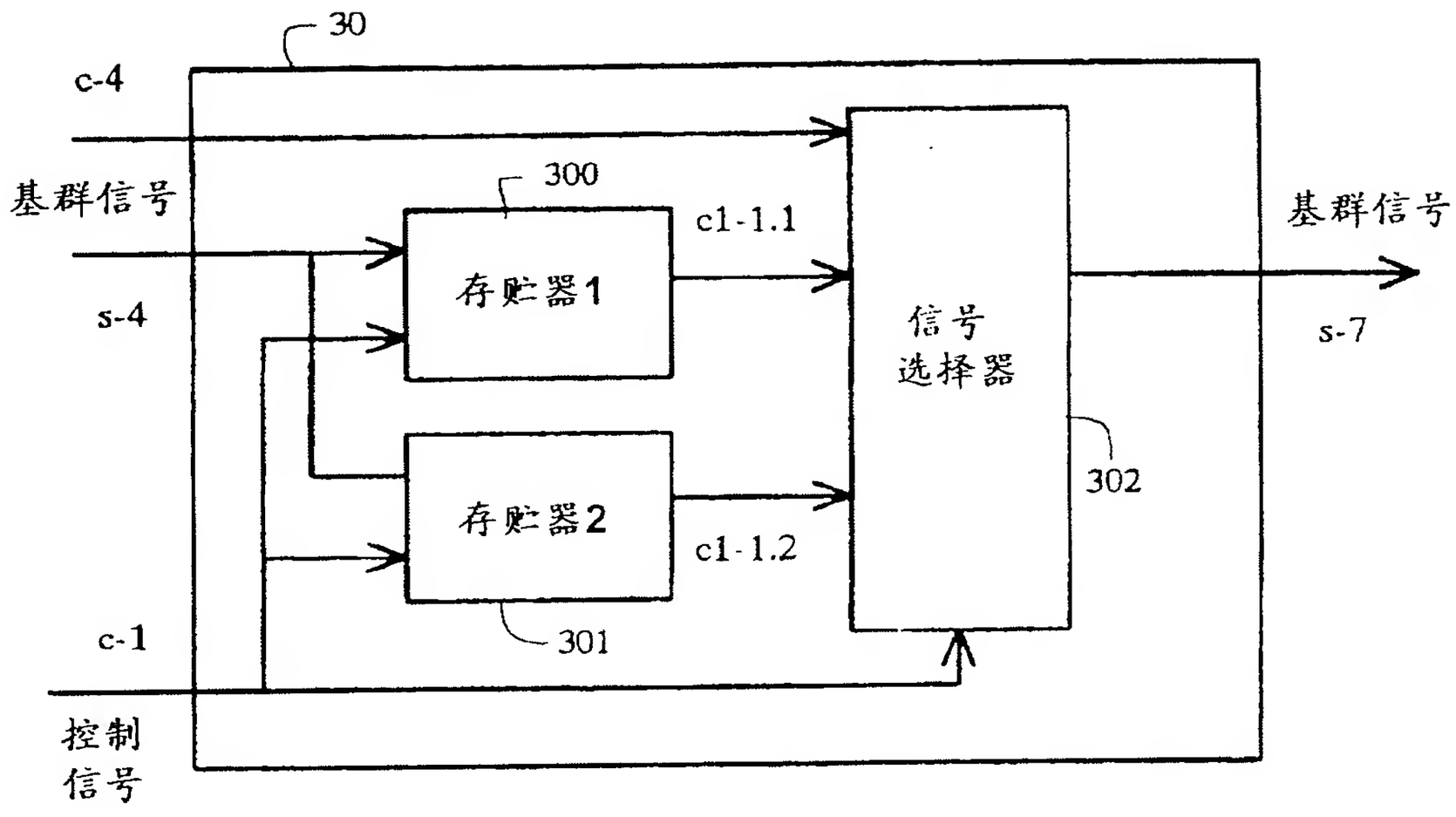

30
c-4
基群信号
300
c1-1.1
基群信号
s-4
存贮器1
信号
选择器
s-7
存贮器2
302
c1-1.2
c-1
301
控制
信号

图 8

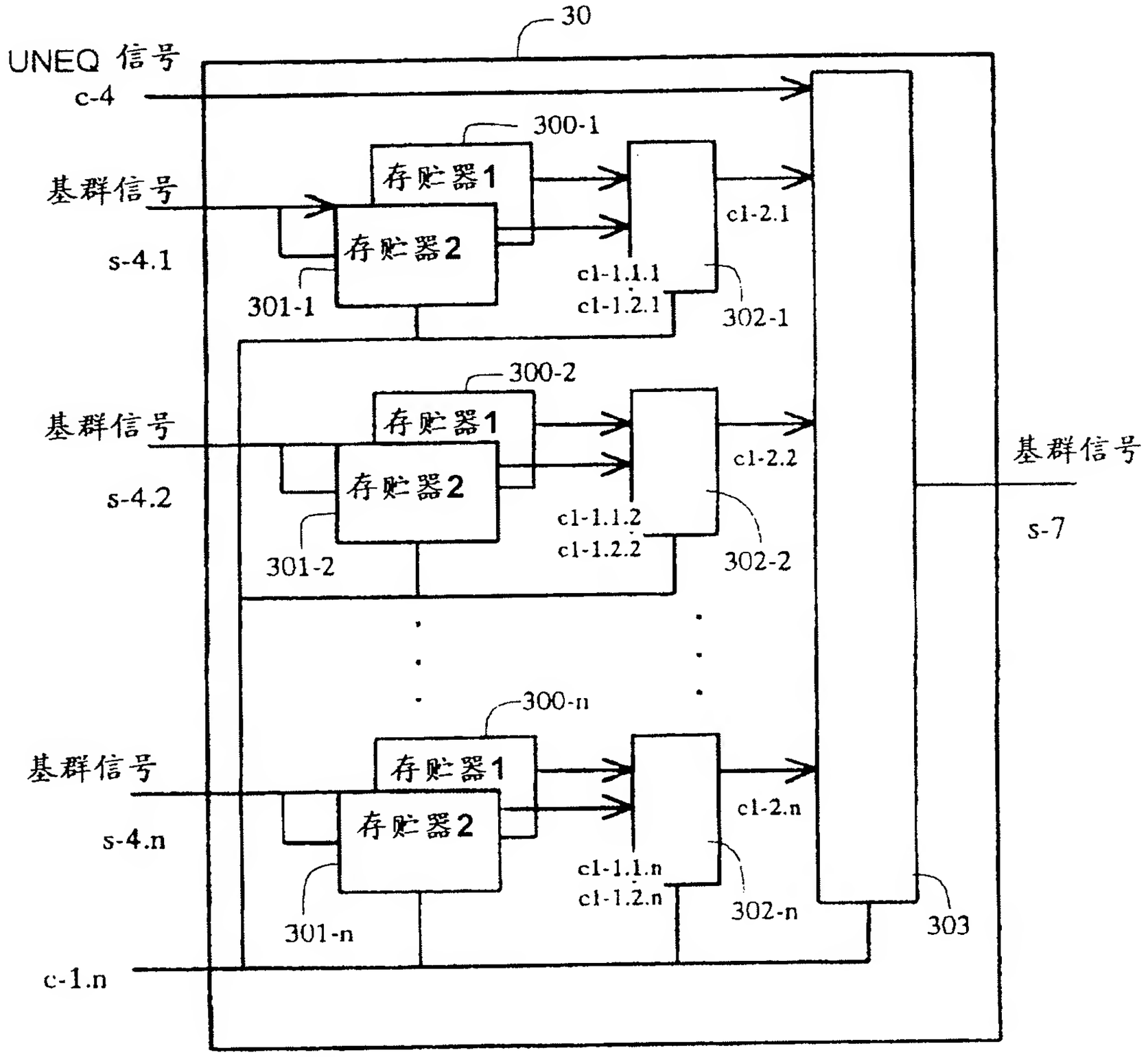

30
UNEQ 信号
c-4
300-1
存贮器1
基群信号
存贮器2
s-4.1
301-1
c1-1.1.1
c1-1.2.1
c1-2.1
302-1
300-2
基群信号
存贮器1
存贮器2
s-4.2
301-2
c1-1.1.2
c1-1.2.2
c1-2.2
302-2
基群信号
s-7
300-n
基群信号
存贮器1
存贮器2
s-4.n
301-n
c1-1.1.n
c1-1.2.n
c1-2.n
302-n
303
c-1.n

图 9

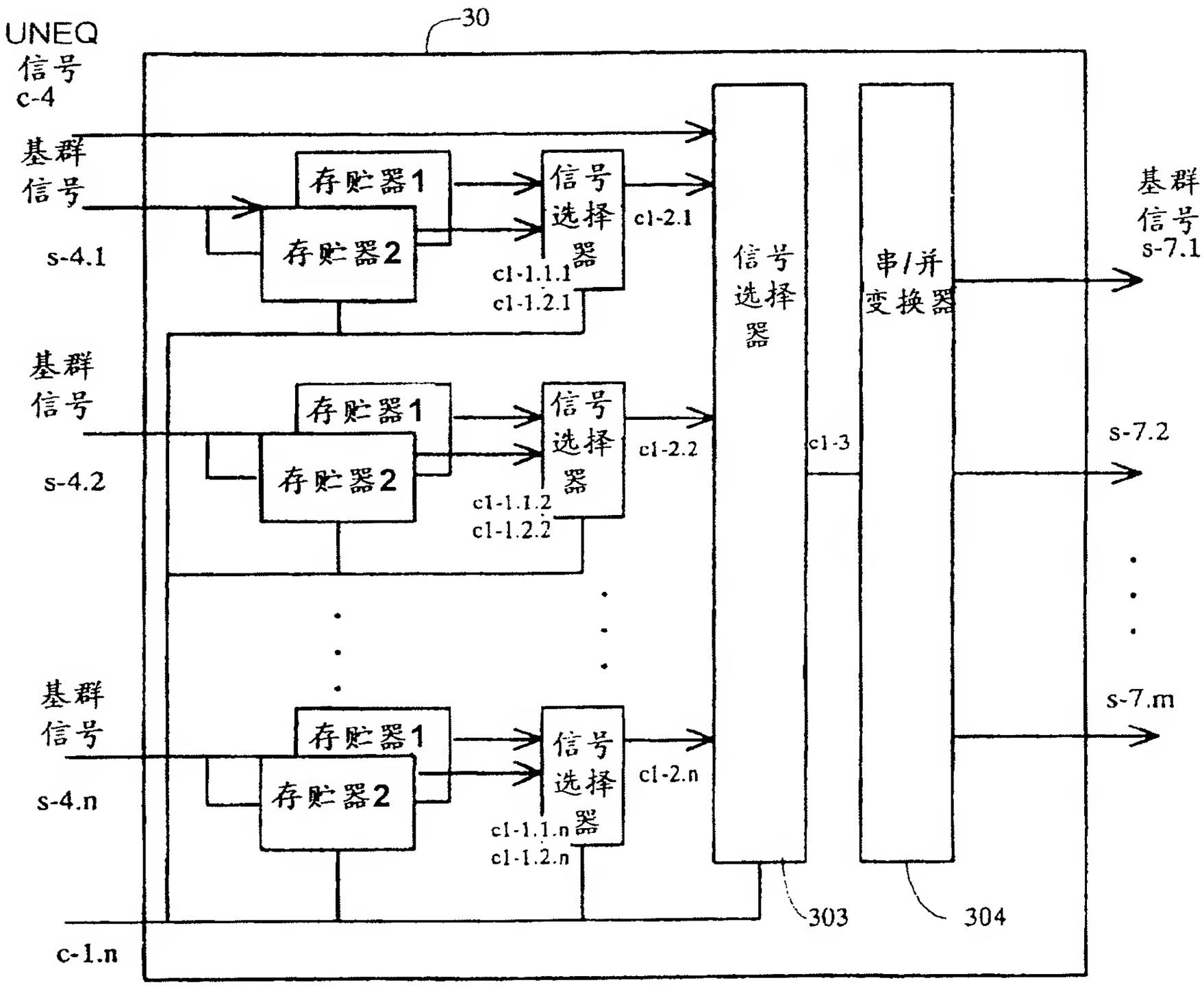

UNEQ
信号
c-4
30
基群
信号
s-4.1
存贮器1
存贮器2
信号
选择
器
c1-1.1.1
c1-1.2.1
c1-2.1
基群
信号
s-4.2
存贮器1
存贮器2
信号
选择
器
c1-1.1.2
c1-1.2.2
c1-2.2
基群
信号
s-4.n
存贮器1
存贮器2
信号
选择
器
c1-1.1.n
c1-1.2.n
c1-2.n
c-1.n
信号
选择
器
c1-3
串/并
变换器
基群
信号
s-7.1
s-7.2
s-7.m
303
304

图 10

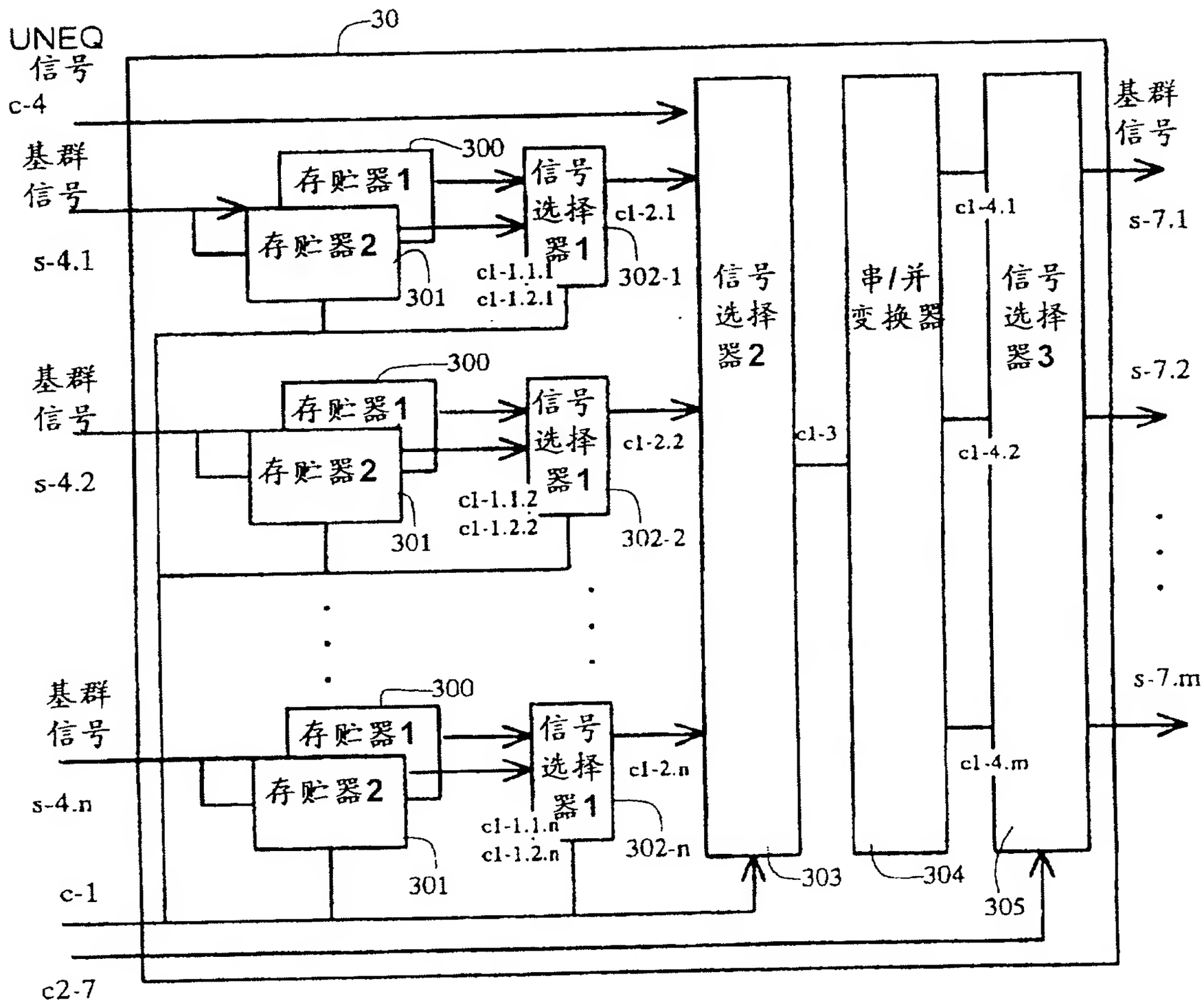

UNEQ
信号
c-4
30
基群
信号
s-4.1
300
存贮器1
存贮器2
301
信号
选择
器1
c1-1.1.1
c1-1.2.1
c1-2.1
302-1
基群
信号
s-4.2
300
存贮器1
存贮器2
301
信号
选择
器1
c1-1.1.2
c1-1.2.2
c1-2.2
302-2
基群
信号
s-4.n
300
存贮器1
存贮器2
301
信号
选择
器1
c1-1.1.n
c1-1.2.n
c1-2.n
302-n
c-1
信号
选择
器2
c1-3
303
串/并
变换器
304
c1-4.1
c1-4.2
c1-4.m
信号
选择
器3
305
基群
信号
s-7.1
s-7.2
s-7.m
c2-7

图 11

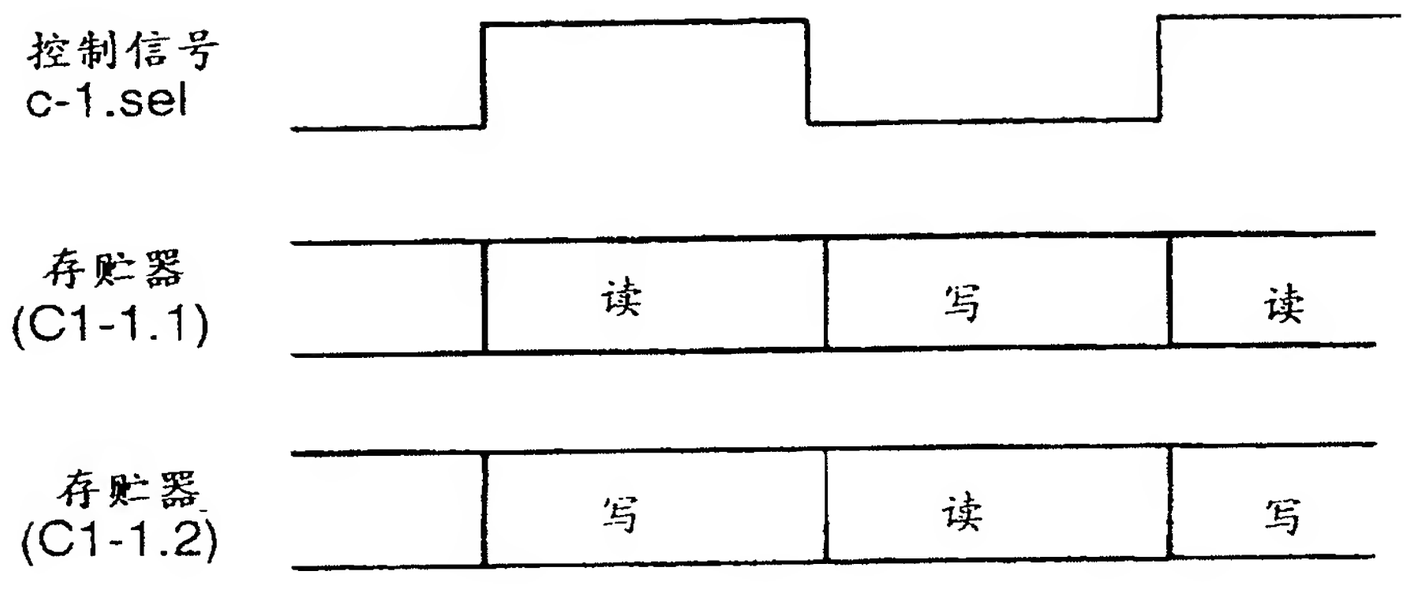


图12

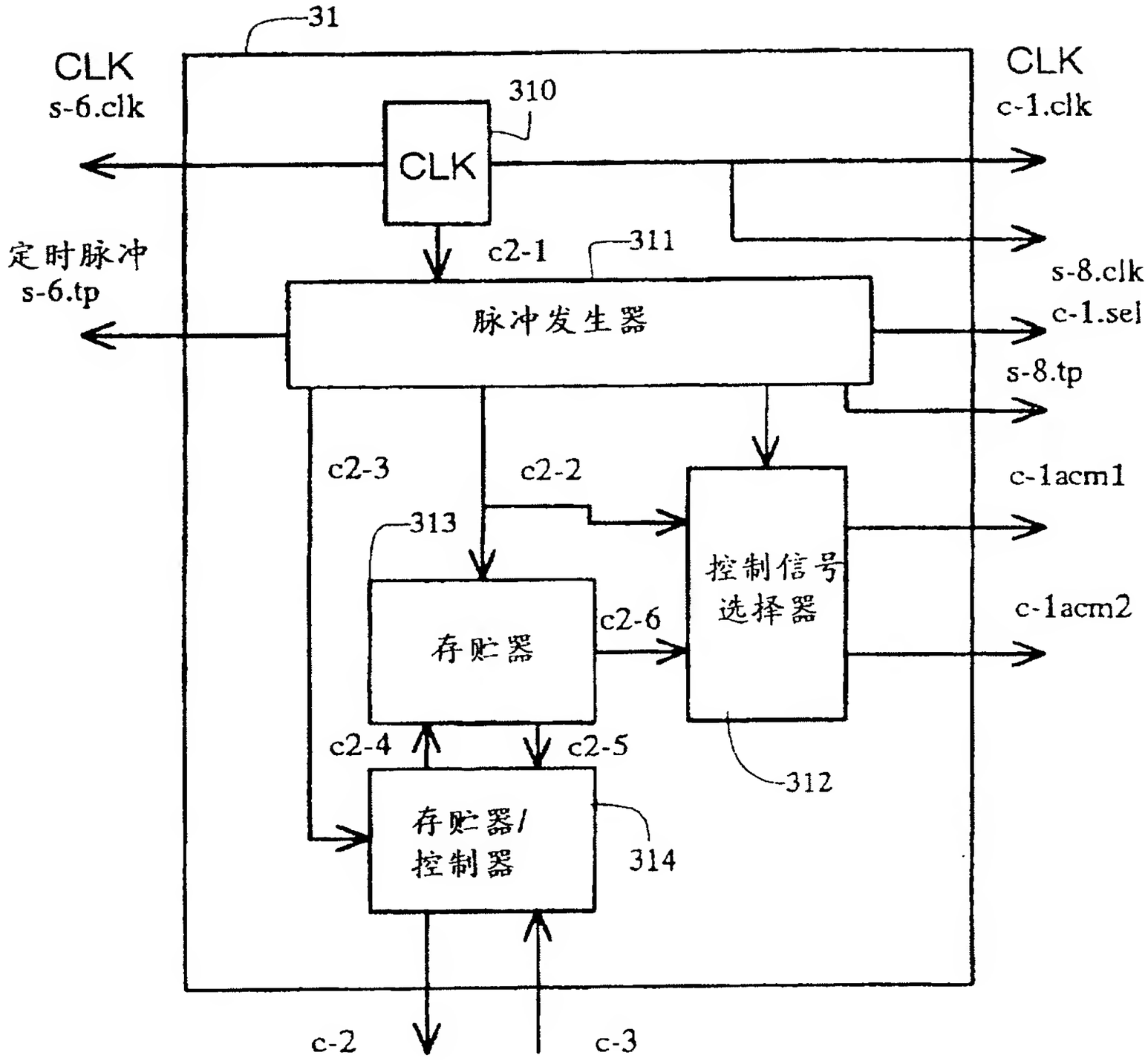

31
CLK
s-6.clk
310
CLK
CLK
c-1.clk
定时脉冲
s-6.tp
c2-1
311
s-8.clk
c-1.sel
脉冲发生器
s-8.tp
c2-3
c2-2
c-1acm1
313
控制信号
选择器
存贮器
c2-6
c-1acm2
c2-4
c2-5
312
存贮器/
控制器
314
c-2
c-3

图 13

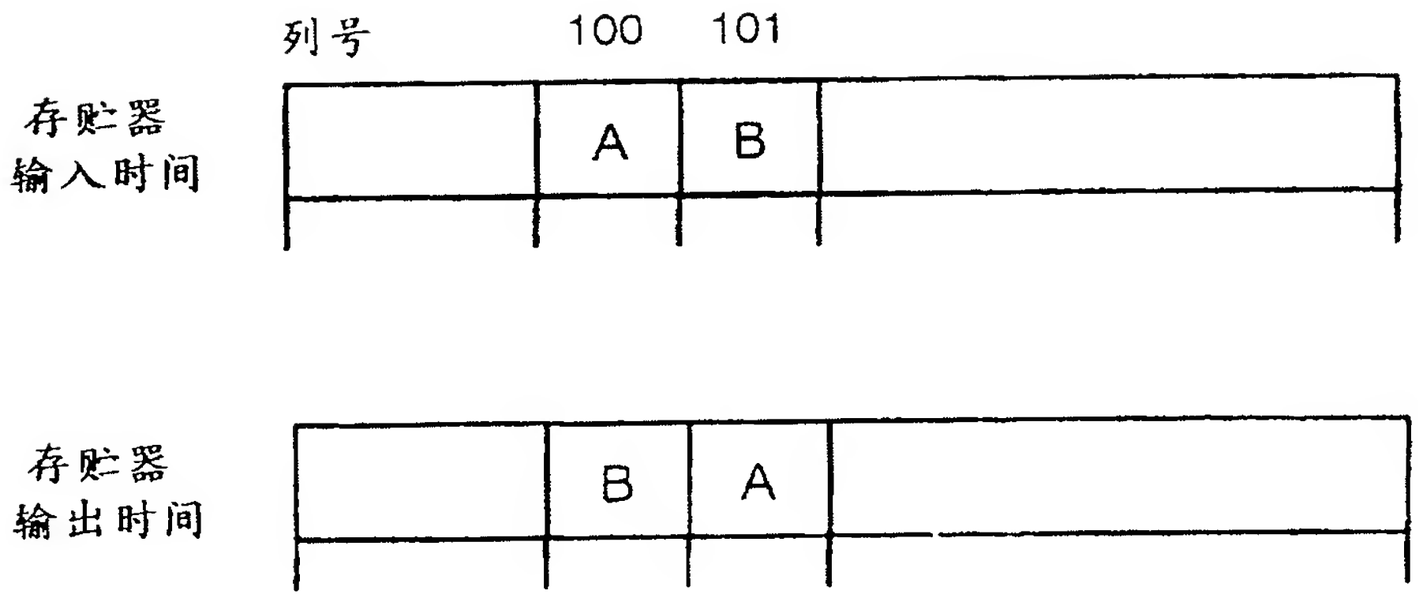


图 14

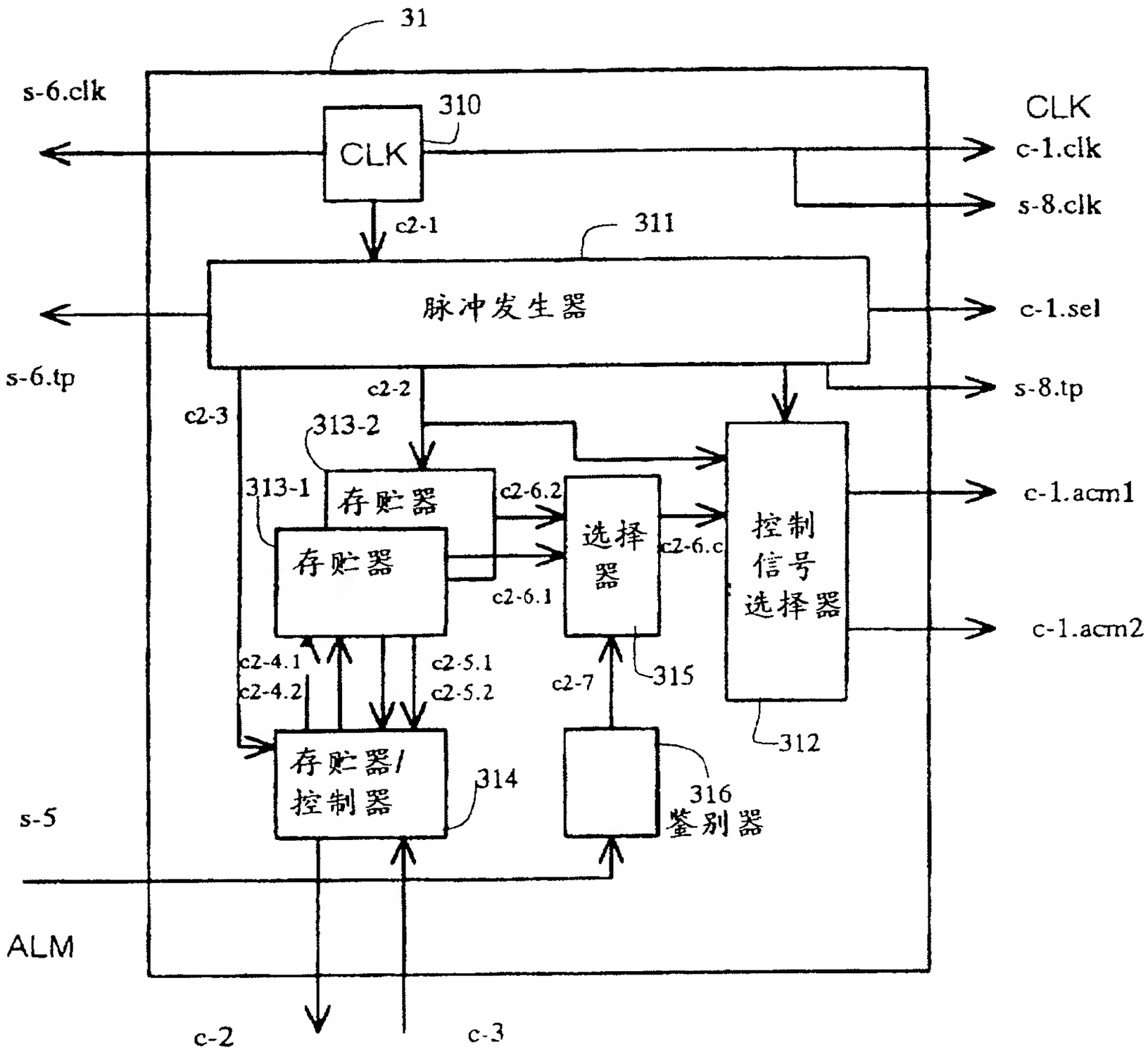

31
s-6.clk
CLK
310
CLK
c-1.clk
s-8.clk
c2-1
311
脉冲发生器
c-1.sel
s-6.tp
s-8.tp
c2-2
c2-3
313-2
313-1
存贮器
存贮器
c2-6.2
c2-6.1
选择器
c2-6.c
控制信号选择器
c-1.acm1
c-1.acm2
c2-4.1
c2-4.2
c2-5.1
c2-5.2
c2-7
315
312
存贮器/控制器
314
316
鉴别器
s-5
ALM
c-2
c-3

图 15

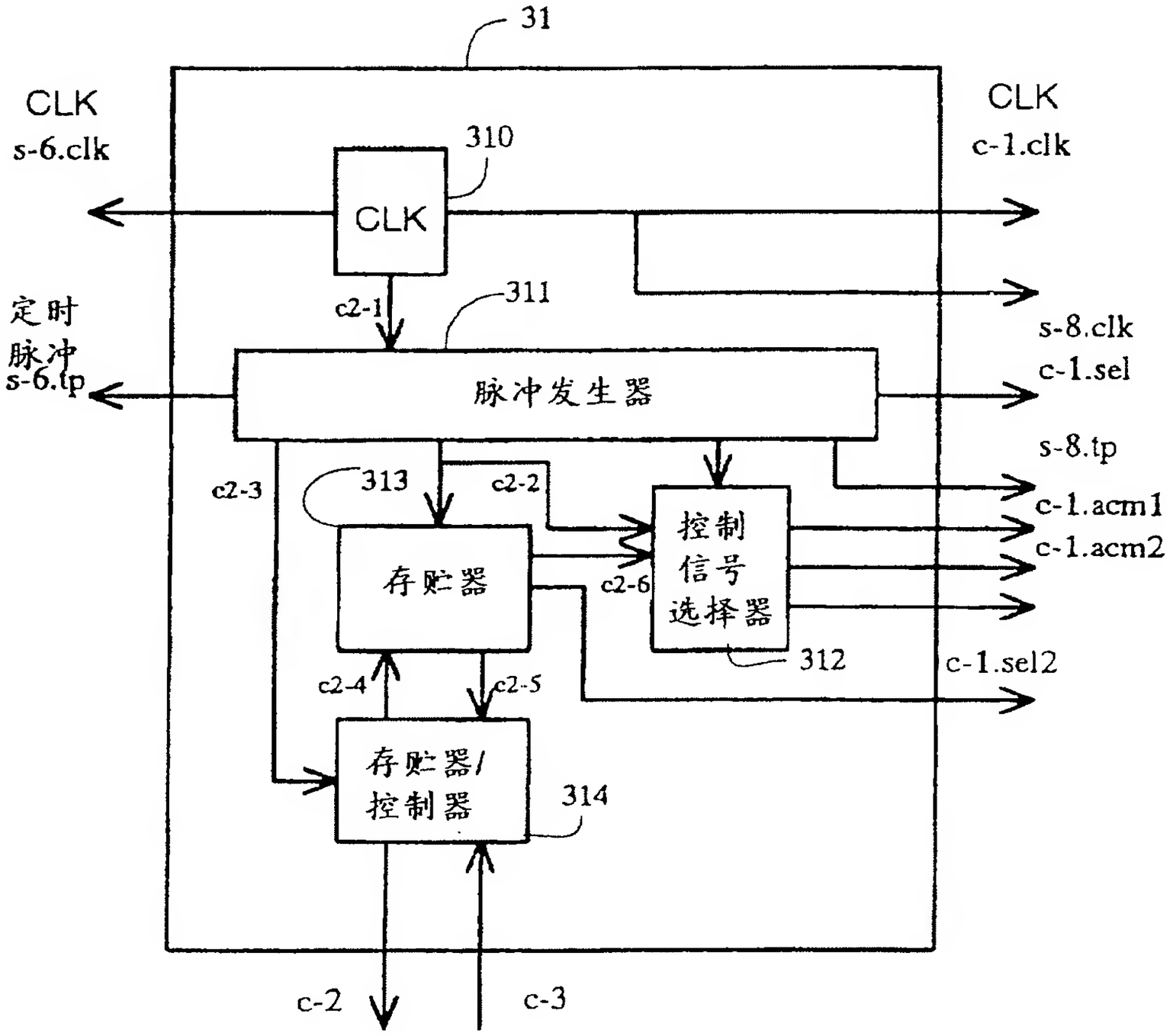

31
CLK
s-6.clk
310
CLK
CLK
c-1.clk
定时
脉冲
s-6.tp
c2-1
311
脉冲发生器
s-8.clk
c-1.sel
s-8.tp
c-1.acm1
c-1.acm2
c-1.sel2
c2-3
313
c2-2
存贮器
c2-6
控制
信号
选择器
312
c2-4
c2-5
存贮器/
控制器
314
c-2
c-3

图16

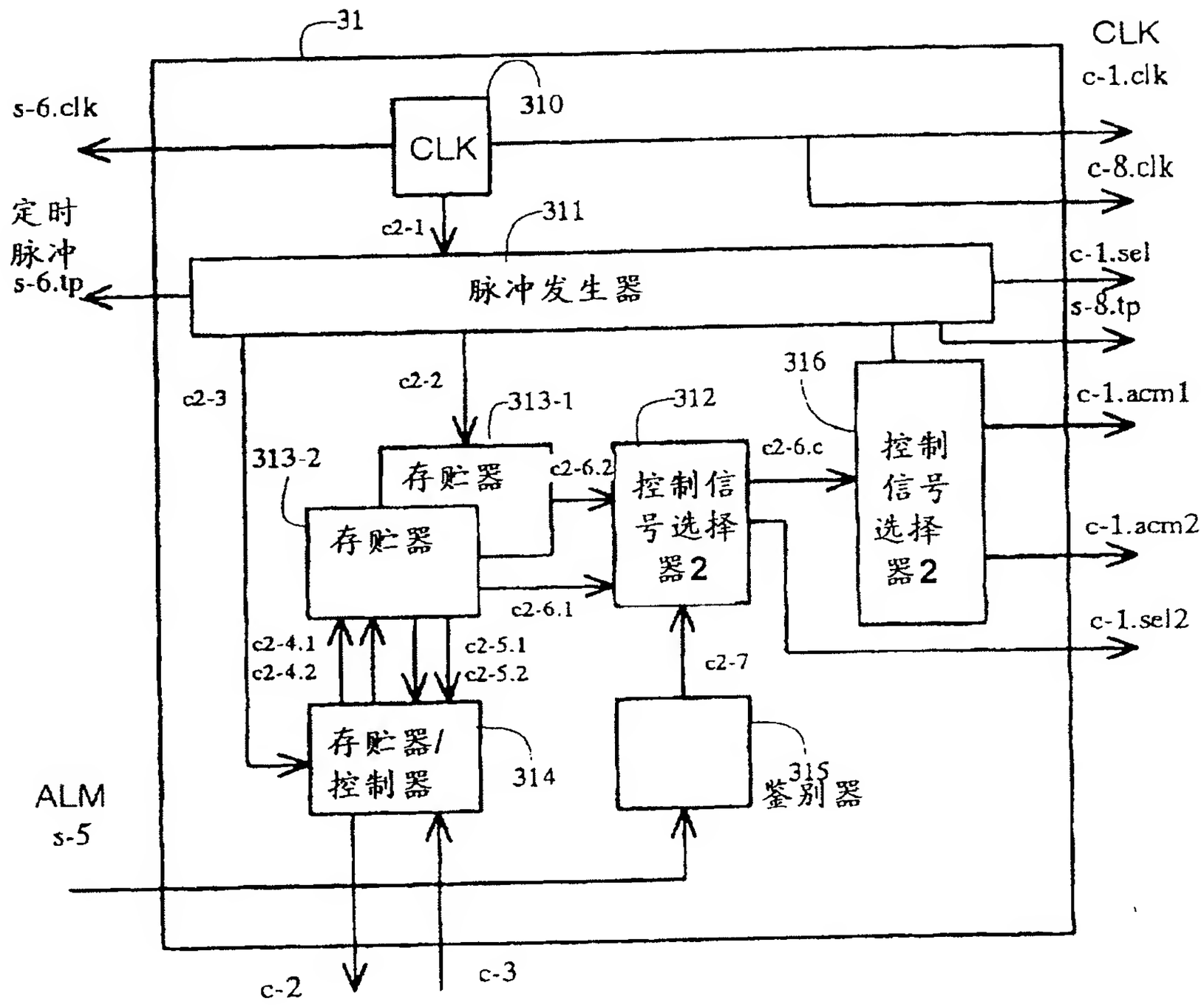

31
CLK
c-1.clk
s-6.clk
310
CLK
c-8.clk
定时
脉冲
s-6.tp
c2-1
311
c-1.sel
脉冲发生器
s-8.tp
316
c2-3
c2-2
313-1
312
c-1.acm1
313-2
存贮器
c2-6.2
控制信号选择器2
c2-6.c
控制信号选择器2
存贮器
c-1.acm2
c2-6.1
c-1.sel2
c2-4.1
c2-4.2
c2-5.1
c2-5.2
c2-7
存贮器/控制器
314
315
鉴别器
ALM
s-5
c-2
c-3

图17

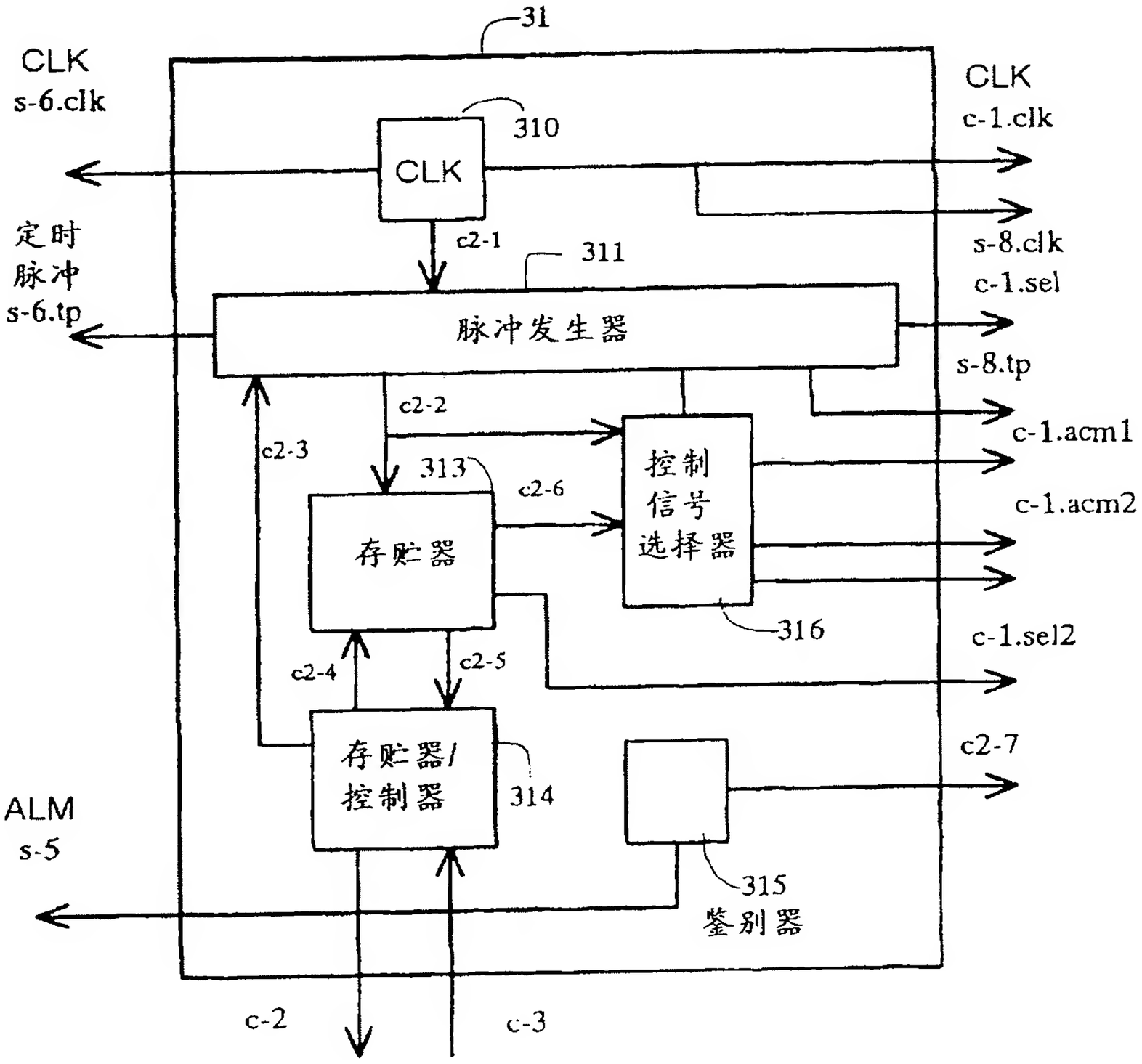

31
CLK
s-6.clk
CLK
c-1.clk
310
CLK
s-8.clk
定时
脉冲
s-6.tp
c2-1
311
c-1.sel
脉冲发生器
s-8.tp
c2-2
c-1.acm1
c2-3
313
c2-6
控制
信号
选择器
c-1.acm2
存贮器
316
c-1.sel2
c2-4
c2-5
存贮器/
控制器
314
c2-7
ALM
s-5
315
鉴别器
c-2
c-3

图 18

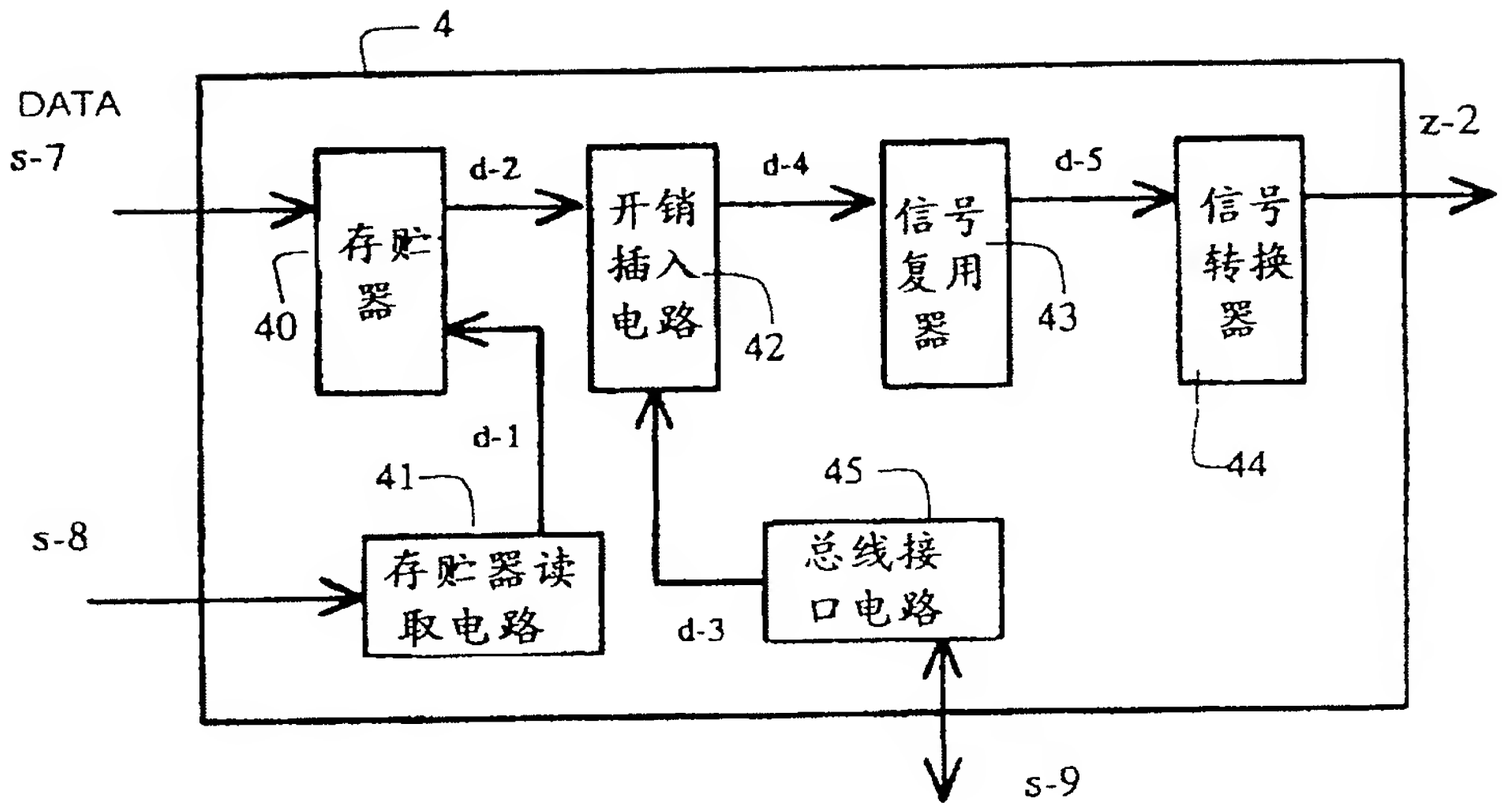

4
DATA
s-7
存贮器
40
d-2
开销插入电路
42
d-4
信号复用器
43
d-5
信号转换器
44
z-2
d-1
41
s-8
存贮器读取电路
d-3
45
总线接口电路
s-9

图19

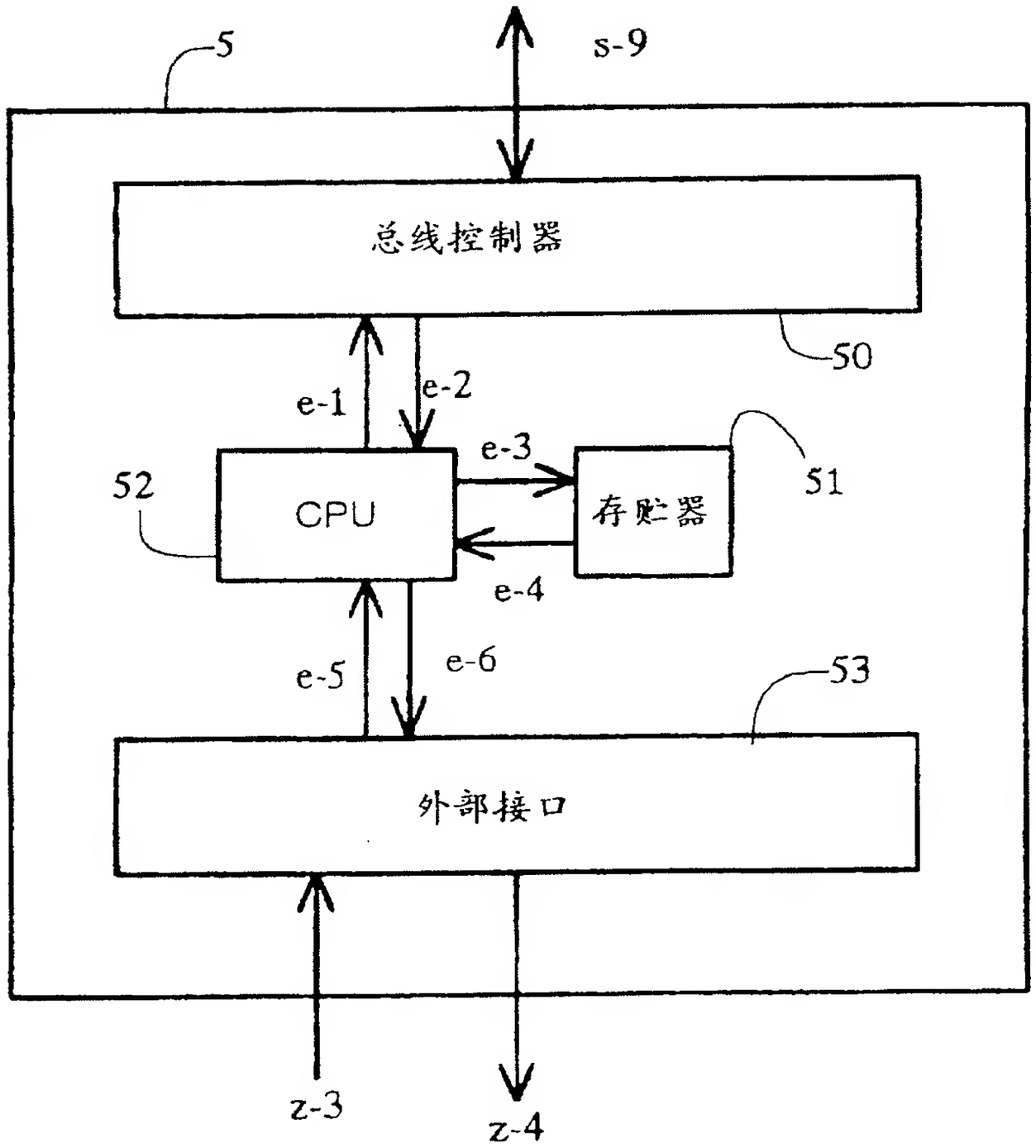


图 20

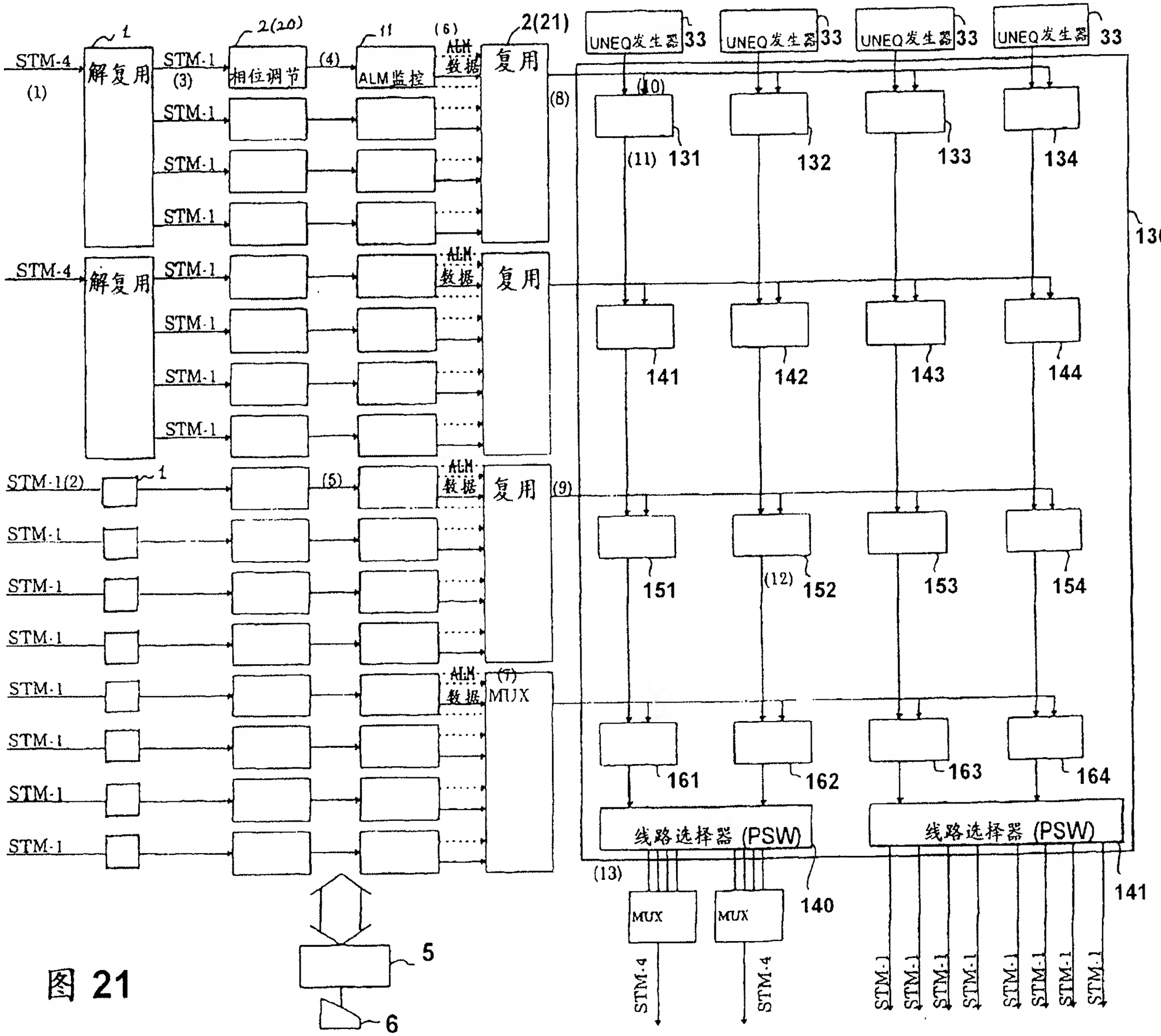

STM-4
(1)
1
解复用
STM-1
(3)
2(20)
相位调节
(4)
11
ALM监控
(6)
ALM数据
2(21)
复用
(8)
UNEQ发生器 33
(10)
(11) 131
132
133
134
130
STM-4
解复用
141
142
143
144
STM-1(2)
(5)
(9)
151
(12) 152
153
154
(7)
MUX
161
162
163
164
线路选择器 (PSW)
(13)
140
141
MUX
STM-4
5
6

图 21

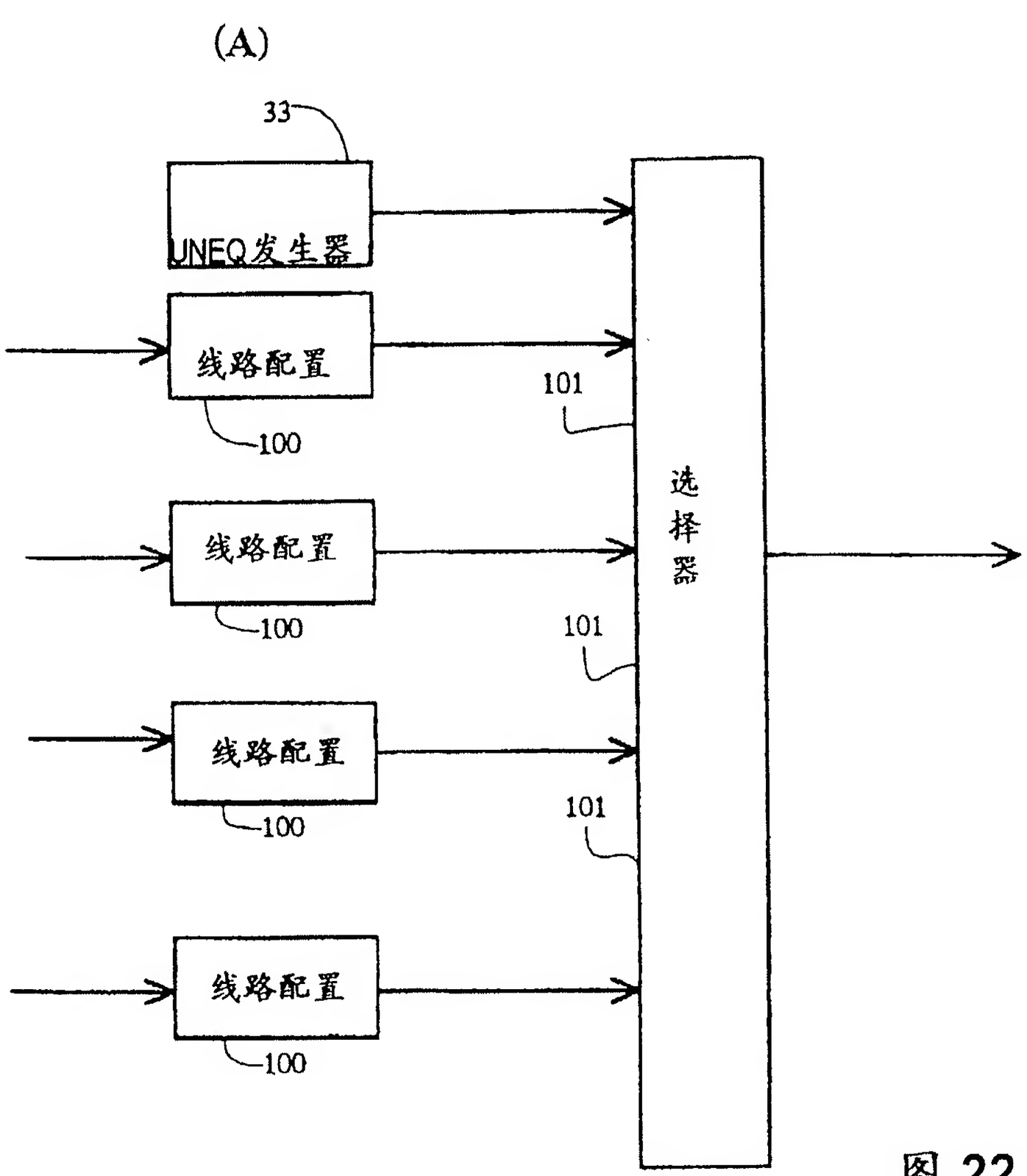

(A)
33
UNEQ发生器
线路配置
100
101
选择器
(B)
33
UNEQ 发生器
直通方向
线路配置
100
102
SEL
131
141
151
161

图 22

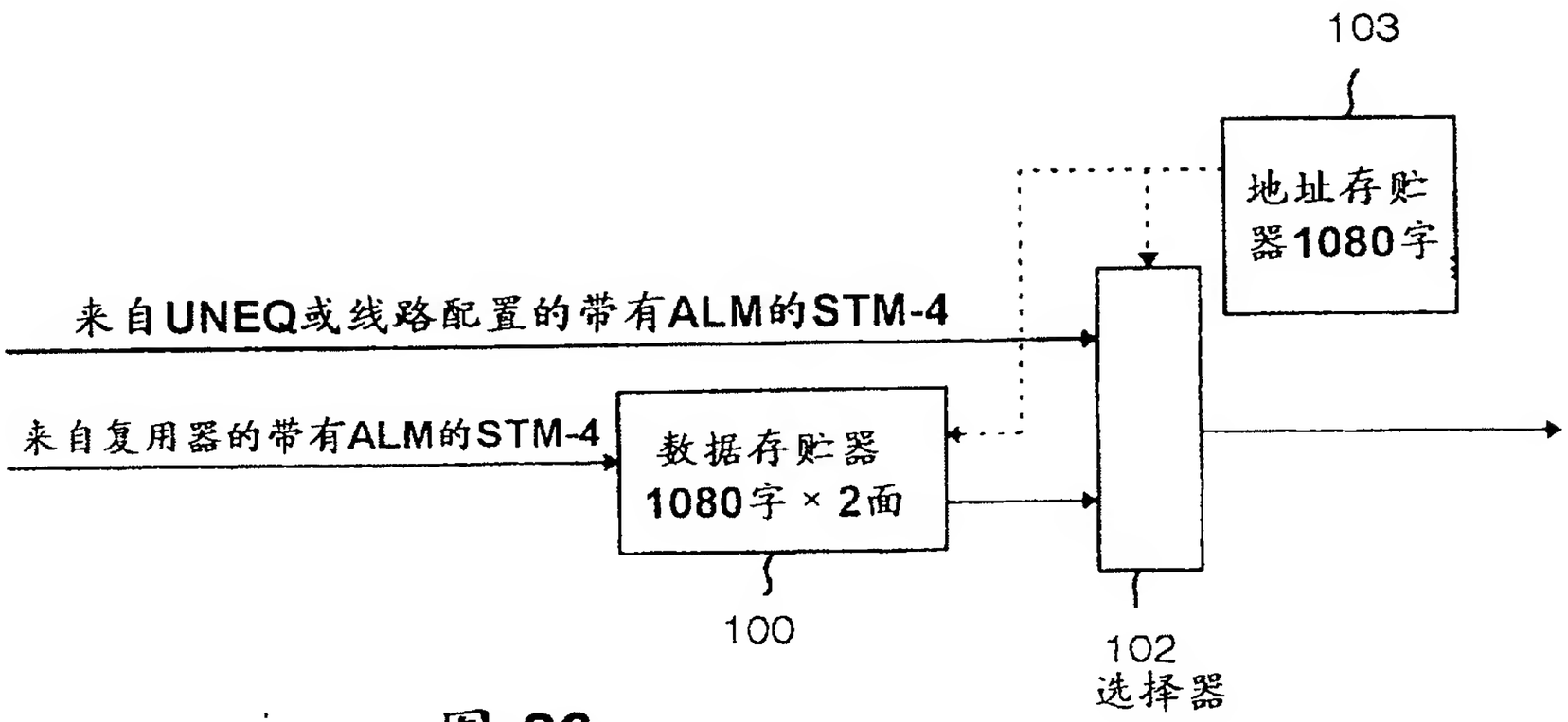

103
地址存贮器1080字
来自UNEQ或线路配置的带有ALM的STM-4
来自复用器的带有ALM的STM-4
数据存贮器
1080字 × 2面
100
102
选择器

图 23

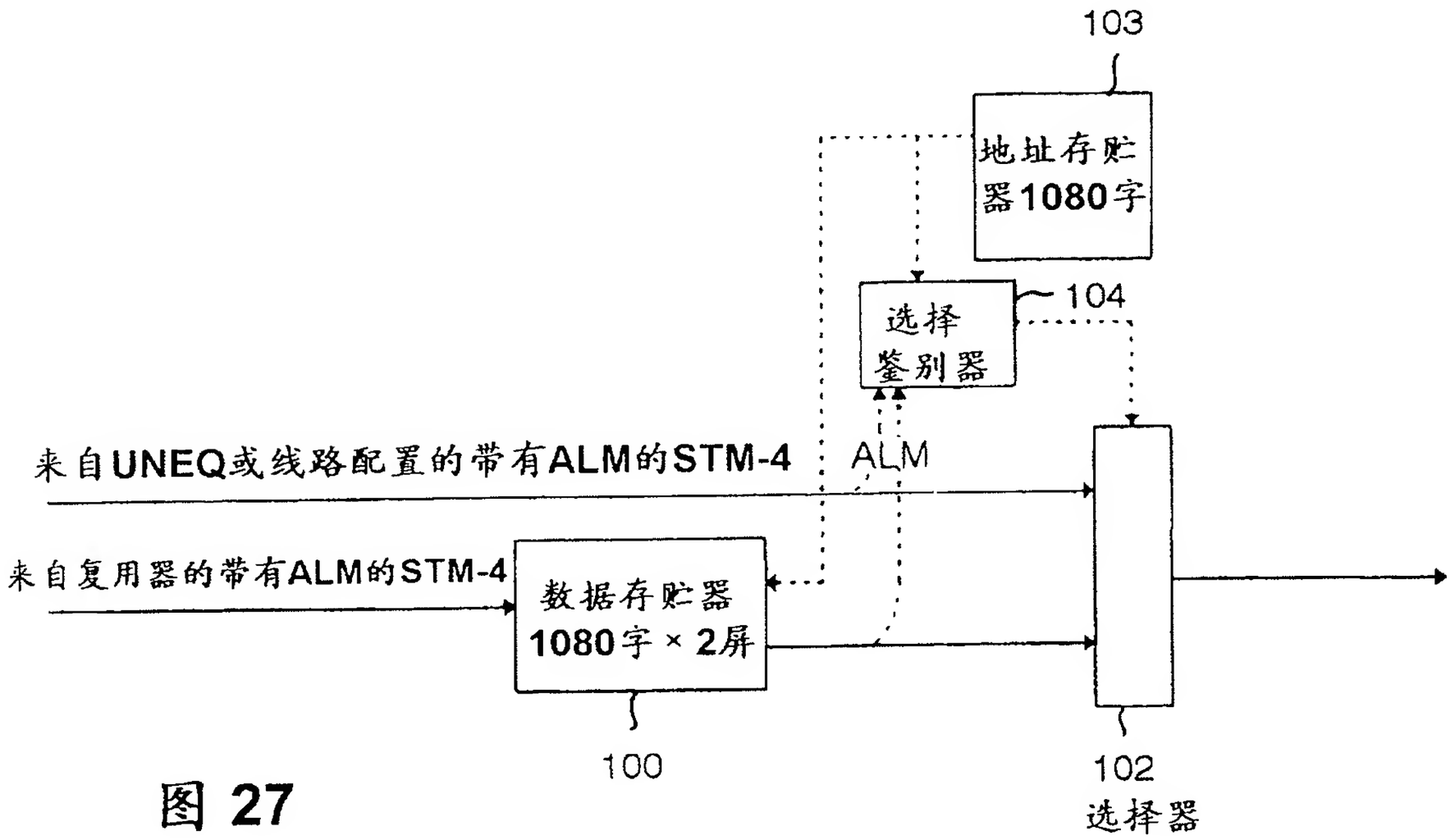

103
地址存贮器1080字
选择
鉴别器
104
来自UNEQ或线路配置的带有ALM的STM-4
ALM
来自复用器的带有ALM的STM-4
数据存贮器
1080字 × 2屏
100
102
选择器

图 27

图 24

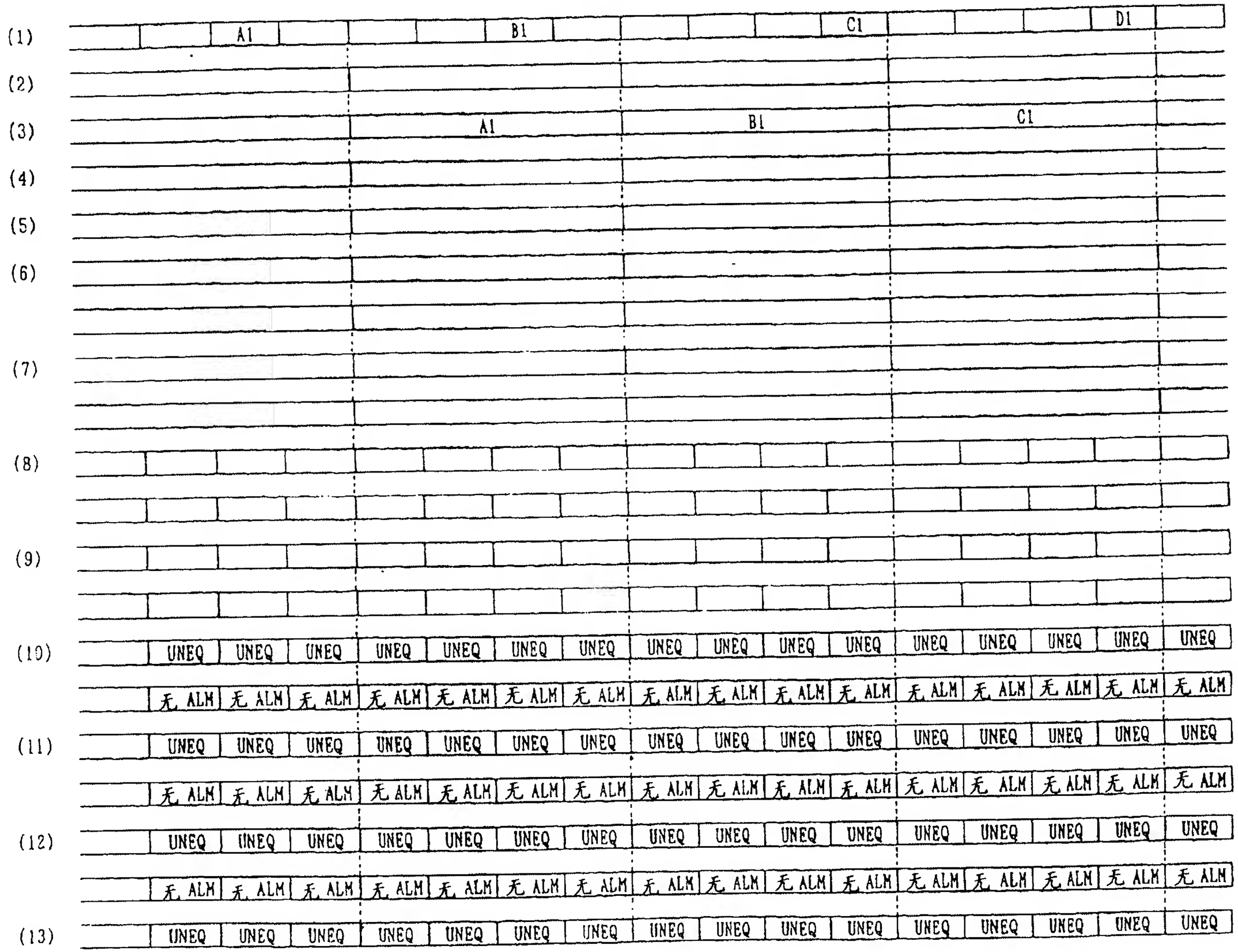
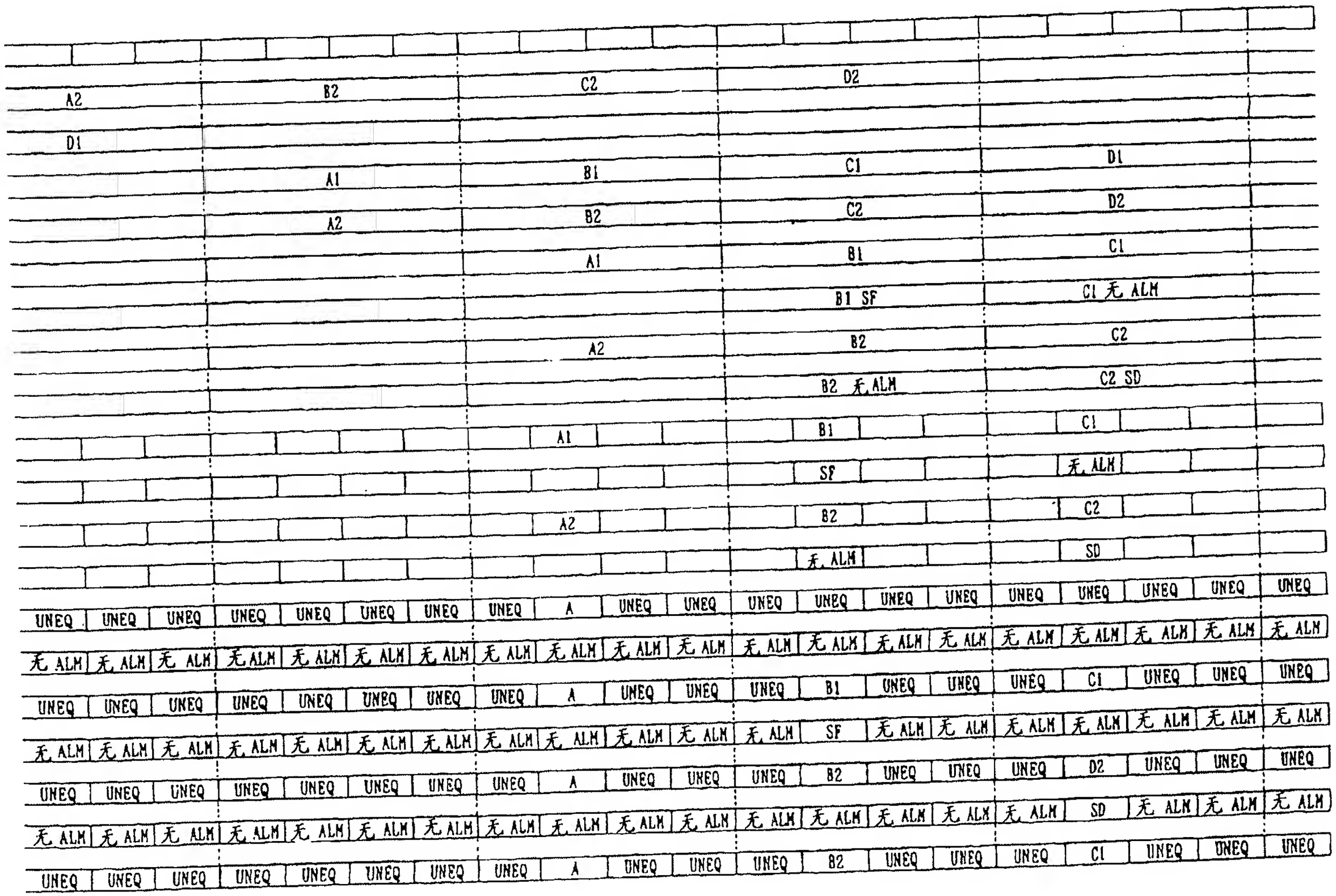

(1)
A1
B1
C1
D1
(2)
(3)
A1
B1
C1
(4)
(5)
(6)
(7)
(8)
(9)
(10)
UNEQ
无 ALM
(11)
UNEQ
无 ALM
(12)
UNEQ
无 ALM
(13)
UNEQ

图25


A2
B2
C2
D2
D1
A1
B1
C1
D1
A2
B2
C2
D2
A1
B1
C1
B1 SF
C1 无 ALM
A2
B2
C2
B2 无 ALM
C2 SD
A1
B1
C1
SF
无 ALM
A2
B2
C2
无 ALM
SD
UNEQ UNEQ UNEQ UNEQ UNEQ UNEQ UNEQ UNEQ A UNEQ UNEQ UNEQ UNEQ UNEQ UNEQ UNEQ UNEQ UNEQ UNEQ UNEQ
无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM
UNEQ UNEQ UNEQ UNEQ UNEQ UNEQ UNEQ UNEQ A UNEQ UNEQ UNEQ B1 UNEQ UNEQ UNEQ C1 UNEQ UNEQ UNEQ
无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM SF 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM
UNEQ UNEQ UNEQ UNEQ UNEQ UNEQ UNEQ UNEQ A UNEQ UNEQ UNEQ B2 UNEQ UNEQ UNEQ D2 UNEQ UNEQ UNEQ
无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM 无 ALM SD 无 ALM 无 ALM 无 ALM
UNEQ UNEQ UNEQ UNEQ UNEQ UNEQ UNEQ UNEQ A UNEQ UNEQ UNEQ B2 UNEQ UNEQ UNEQ C1 UNEQ UNEQ UNEQ

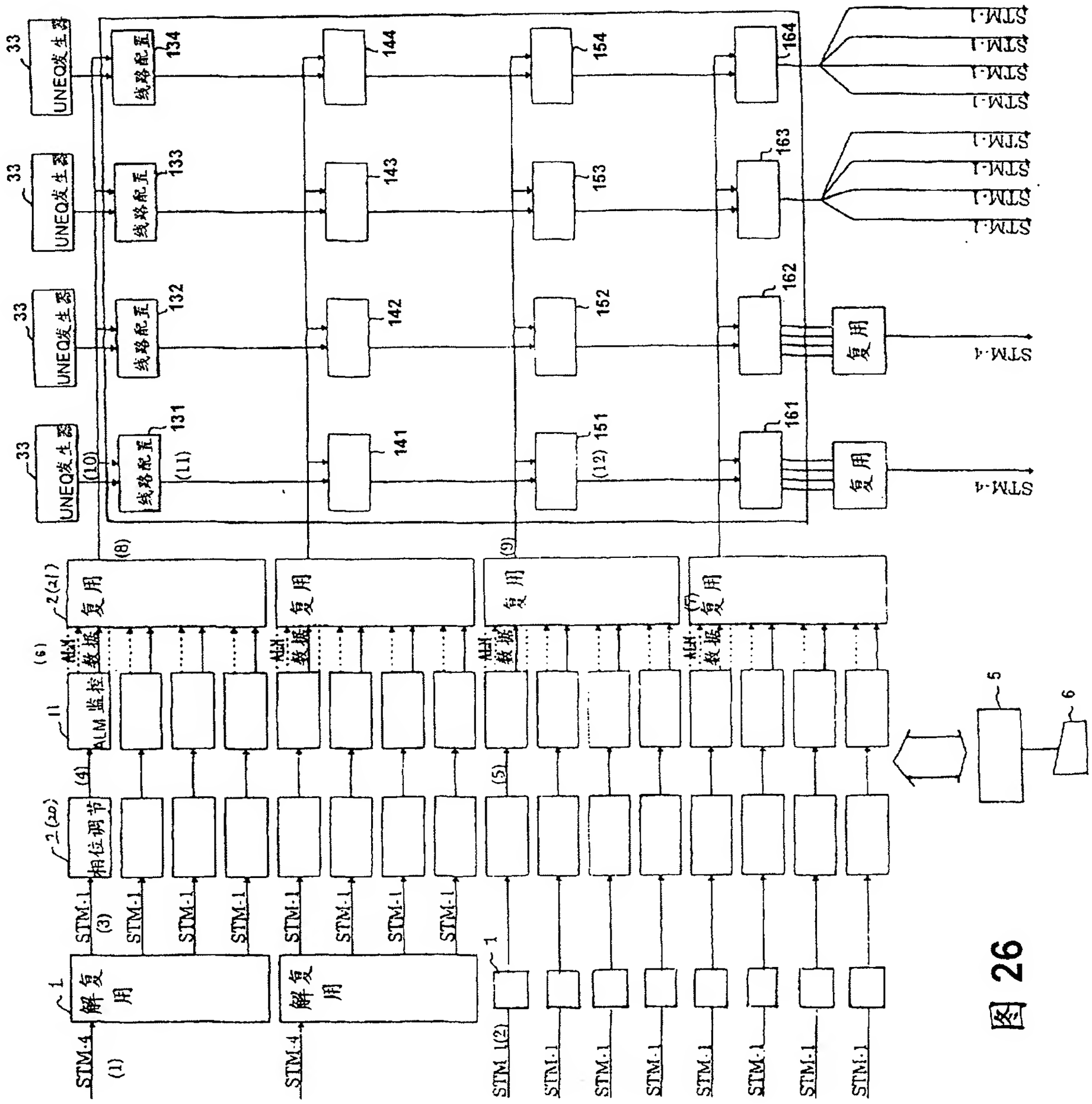

解复用
STM-4
(1)
STM-1
(3)
相位调节
2(20)
(4)
ALM 监控
11
(6)
ALM 数据
复用
2(21)
(8)
(9)
(7)
(10)
(11)
(12)
STM-1(2)
1
5
6
UNEQ发生器
33
线路配置
131
132
133
134
141
142
143
144
151
152
153
154
161
162
163
164
复用
STM-4
STM-1

图 26

(3)	(1)	直通 ALM	存贮器 ALM	选择信号
没有冗余	直通	×	×	直通
没有冗余	数据存贮器	×	×	数据存贮器
冗余	×	无 ALM	无 ALM	保持前行状态
冗余	×	无 ALM	SD	直通
冗余	×	无 ALM	SF	直通
冗余	×	SD	SD	保持前行状态
冗余	×	SD	SF	
冗余	×	SF	SF	保持前行状态

×：不管

图 28

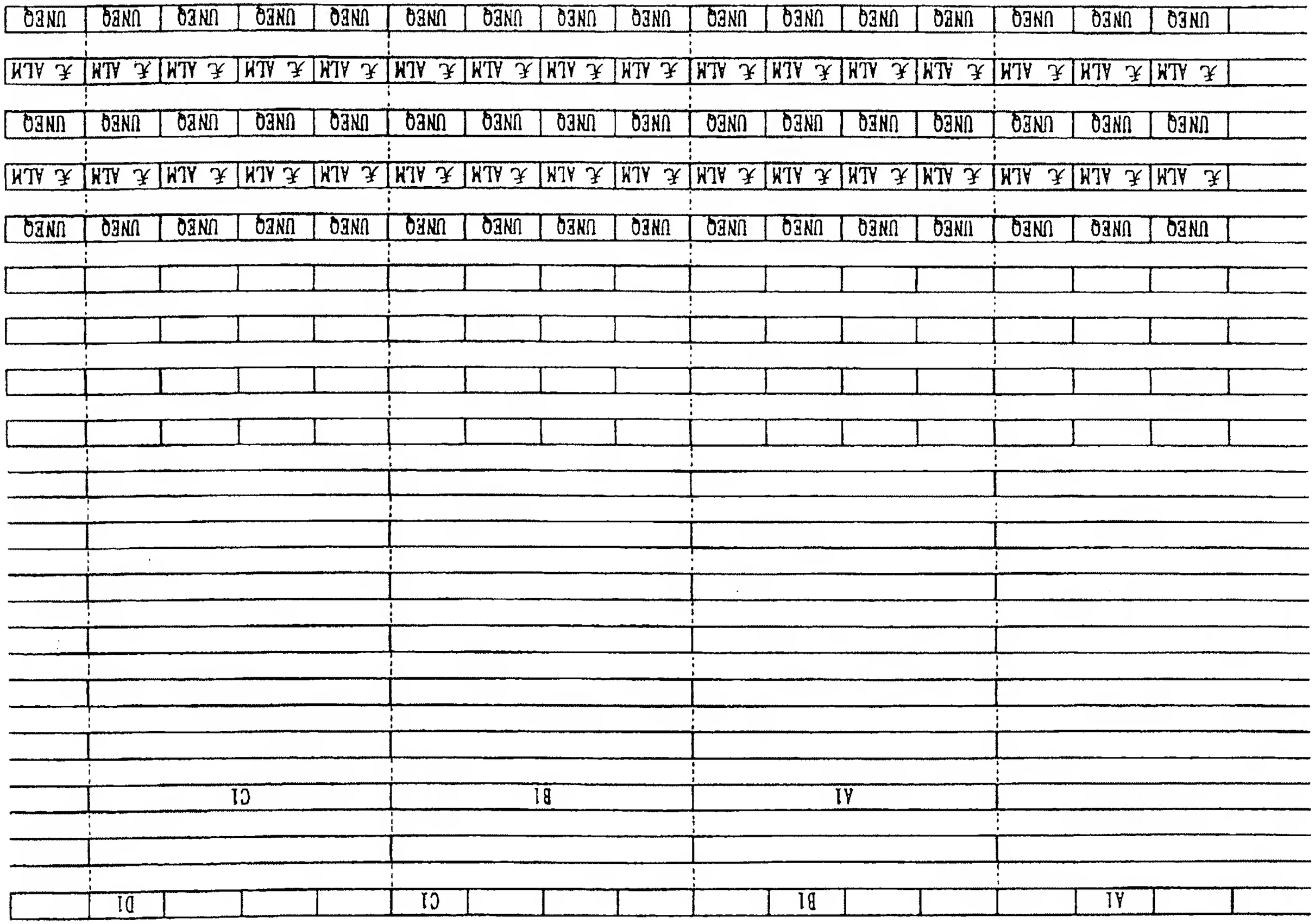


Fig 29

图 30

A2			B2				C2				D2								
D1																			
			A1				B1				C1				D1				
			A2				B2				C2				D2				
							A1				B1				C1				
											B1 SF				C1 无 ALM				
							A2				B2				C2				
											B2 无 ALM				C2 SD				
								A1				B1				C1			
												SF				无 ALM			
								A2				B2				C2			
												无 ALM				SD			
UNEQ	UNEQ	UNEQ	UNEQ	UNEQ	UNEQ	UNEQ	UNEQ	A	UNEQ	UNEQ	UNEQ	UNEQ	UNEQ	UNEQ	UNEQ	UNEQ	UNEQ	UNEQ	UNEQ
无ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM
UNEQ	UNEQ	UNEQ	UNEQ	UNEQ	UNEQ	UNEQ	UNEQ	A	UNEQ	UNEQ	UNEQ	B1	UNEQ	UNEQ	UNEQ	D1	UNEQ	UNEQ	UNEQ
无ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	SF	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM
UNEQ	UNEQ	UNEQ	UNEQ	UNEQ	UNEQ	UNEQ	UNEQ	A	UNEQ	UNEQ	UNEQ	B2	UNEQ	UNEQ	UNEQ	D1	UNEQ	UNEQ	UNEQ

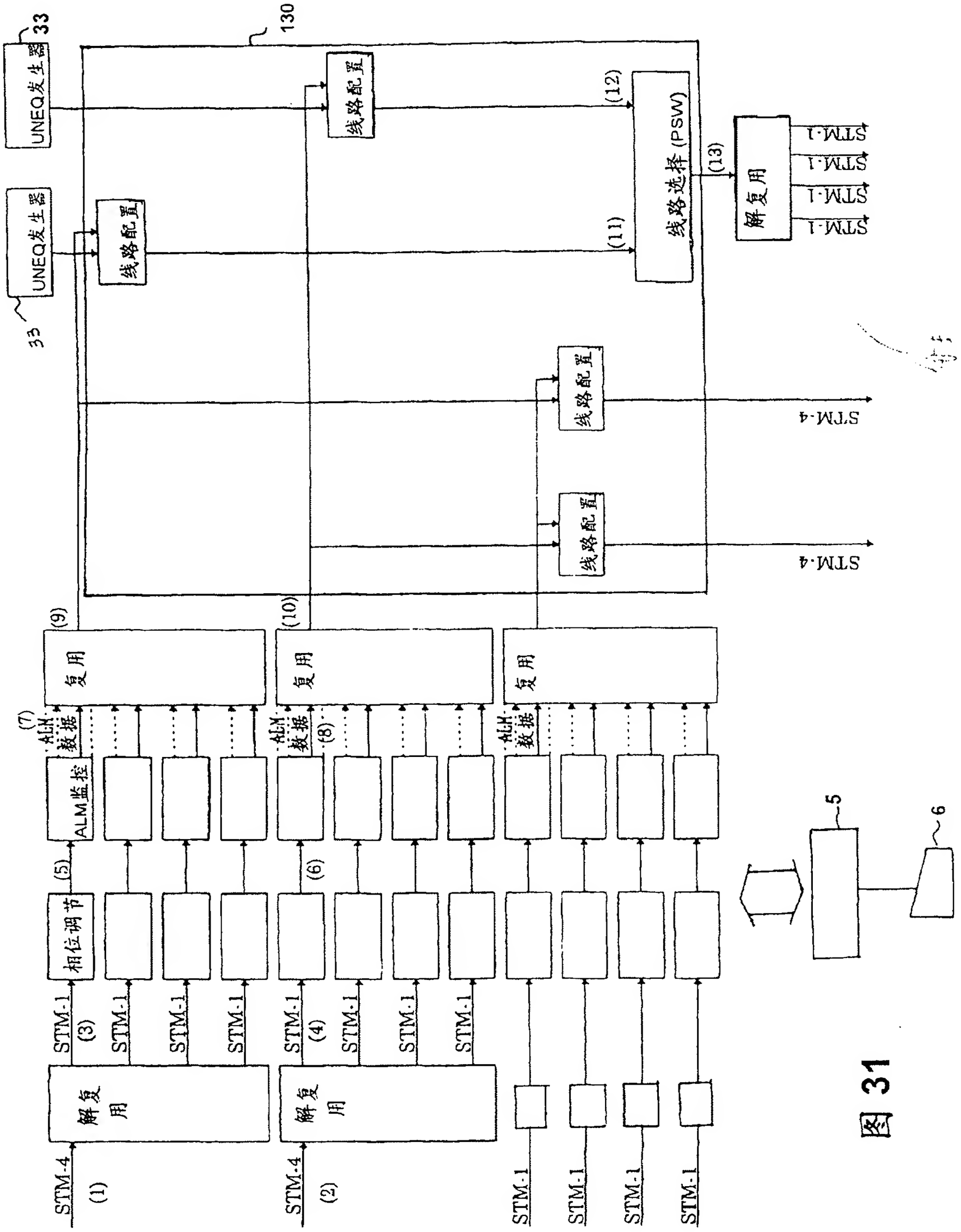

STM-1
STM-1
STM-1
STM-1
解复用
(13)
线路选择 (PSW)
(12)
(11)
线路配置
线路配置
UNEQ发生器
UNEQ发生器
33
130
33
STM-4
STM-4
线路配置
线路配置
(9)
(10)
复用
复用
复用
(7)
(8)
ALM数据
ALM数据
ALM数据
ALM监控
(5)
(6)
相位调节
STM-1
(3)
(4)
STM-1
STM-1
STM-1
STM-1
STM-1
STM-1
STM-1
STM-1
解复用
解复用
STM-4
(1)
STM-4
(2)
STM-1
STM-1
STM-1
STM-1
5
6

图 31

图 32

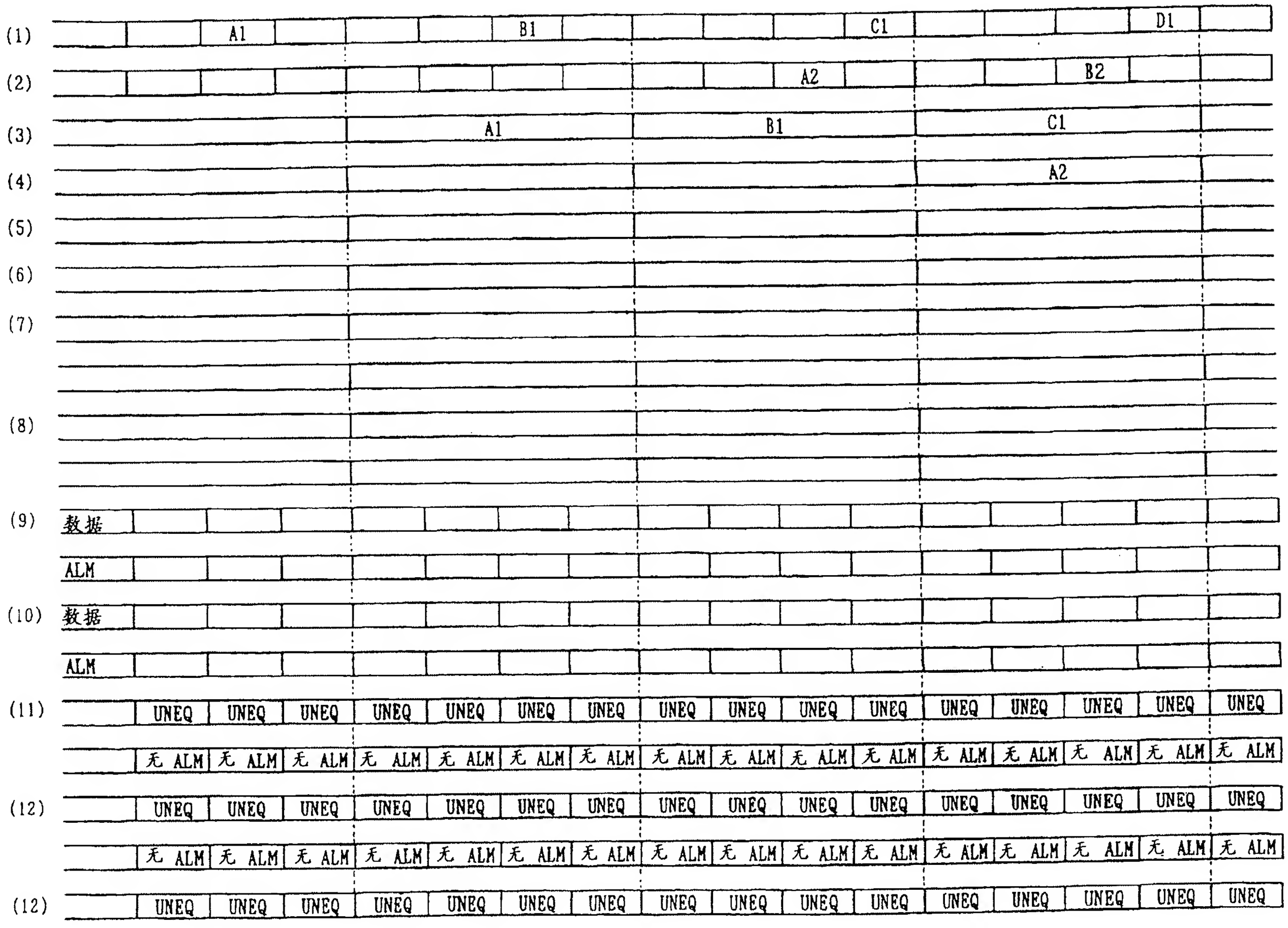

(1)
A1
B1
C1
D1
(2)
A2
B2
(3)
A1
B1
C1
(4)
A2
(5)
(6)
(7)
(8)
(9)
数据
ALM
(10)
数据
ALM
(11)
UNEQ
无 ALM
(12)
UNEQ
无 ALM
(12)
UNEQ

图 33

		C2				D2												
D1																		
B2			C2				D2											
A1			B1				C1				D1				D1			
A2			B2				C2				D2				D2			
			A1				B1				C1				D1			
							B1 SF				C1 SD				D1 无 ALM			
			A2				B2				C2				D2			
							B2 无 ALM				C2 SD				D2 SD			
				A1				B1				C1				D1		
								SF				SD				无 ALM		
				A2				B2				C2				D2		
								无 ALM				SD				SD		
UNEQ	UNEQ	UNEQ	UNEQ	A	UNEQ	UNEQ	UNEQ	D1	UNEQ	UNEQ	UNEQ	C1	UNEQ	UNEQ	UNEQ	B1	UNEQ	UNEQ	UNEQ
无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	SD	无 ALM	无 ALM	无 ALM	SF	无 ALM	无 ALM	无 ALM
UNEQ	UNEQ	UNEQ	UNEQ	A	UNEQ	UNEQ	UNEQ	D2	UNEQ	UNEQ	UNEQ	B2	UNEQ	UNEQ	UNEQ	C2	UNEQ	UNEQ	UNEQ
无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	SD	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	无 ALM	SD	无 ALM	无 ALM	无 ALM
UNEQ	UNEQ	UNEQ	UNEQ	A	UNEQ.	UNEQ	UNEQ	D1	UNEQ	UNEQ	UNEQ	B2	UNEQ	UNEQ	UNEQ	C2	UNEQ	UNEQ	UNEQ

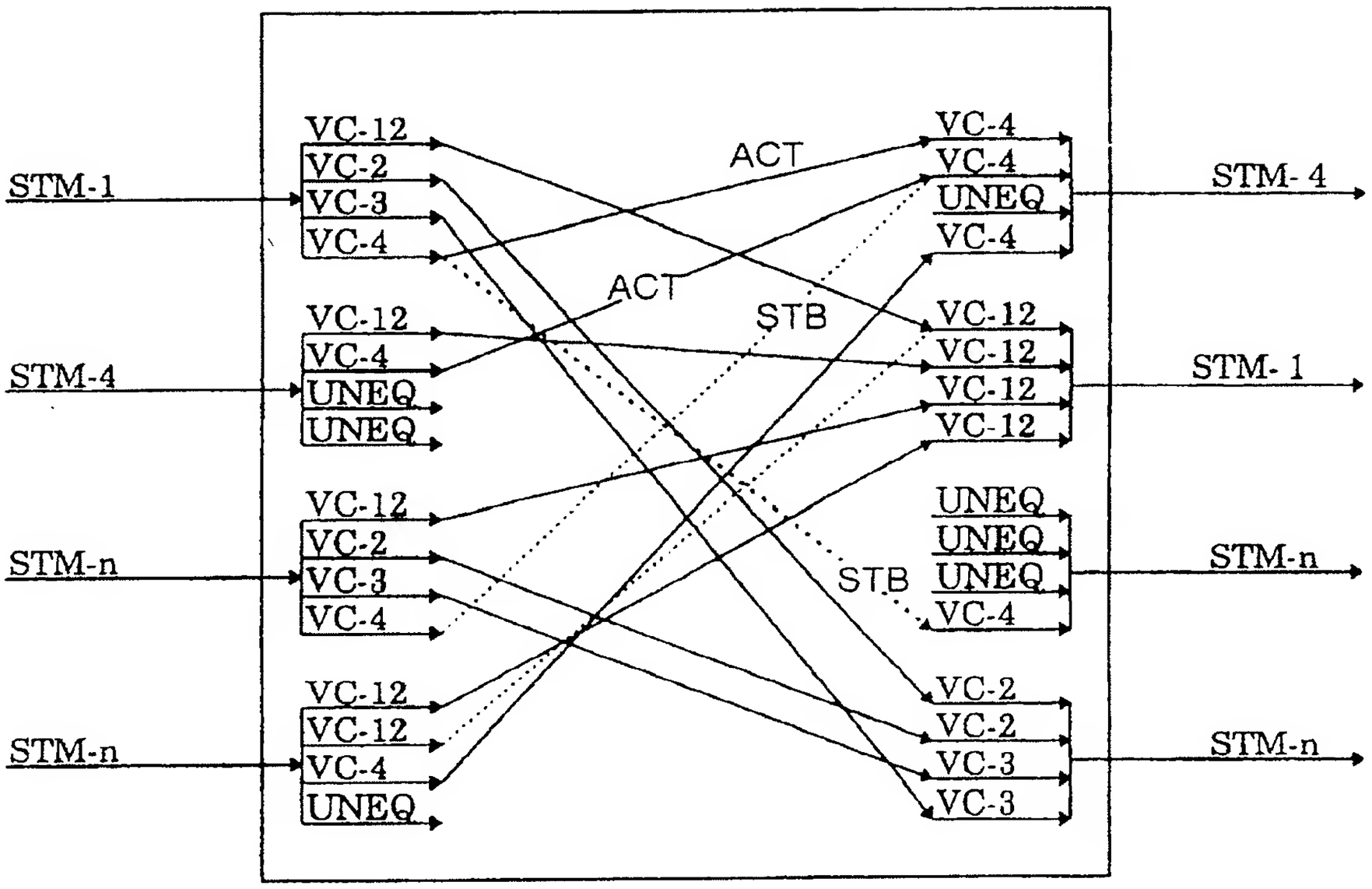

STM-1
STM-4
STM-n
STM-n
VC-12
VC-2
VC-3
VC-4
VC-12
VC-4
UNEQ
UNEQ
VC-12
VC-2
VC-3
VC-4
VC-12
VC-12
VC-4
UNEQ
ACT
ACT
STB
STB
VC-4
VC-4
UNEQ
VC-4
VC-12
VC-12
VC-12
VC-12
UNEQ
UNEQ
UNEQ
VC-4
VC-2
VC-2
VC-3
VC-3
STM- 4
STM- 1
STM-n
STM-n

图 34

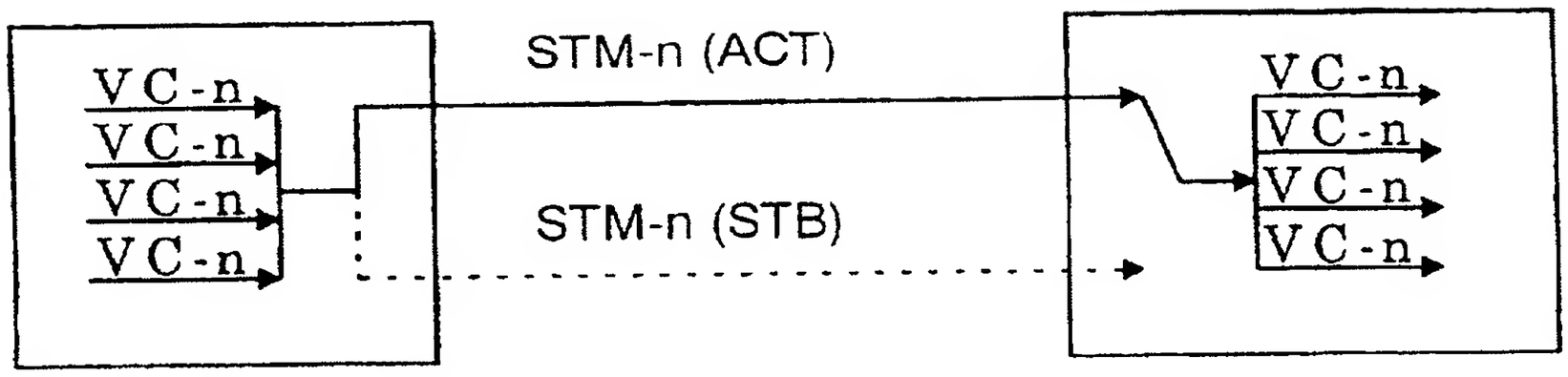

VC-n
VC-n
VC-n
VC-n
STM-n (ACT)
STM-n (STB)
VC-n
VC-n
VC-n
VC-n

图 35

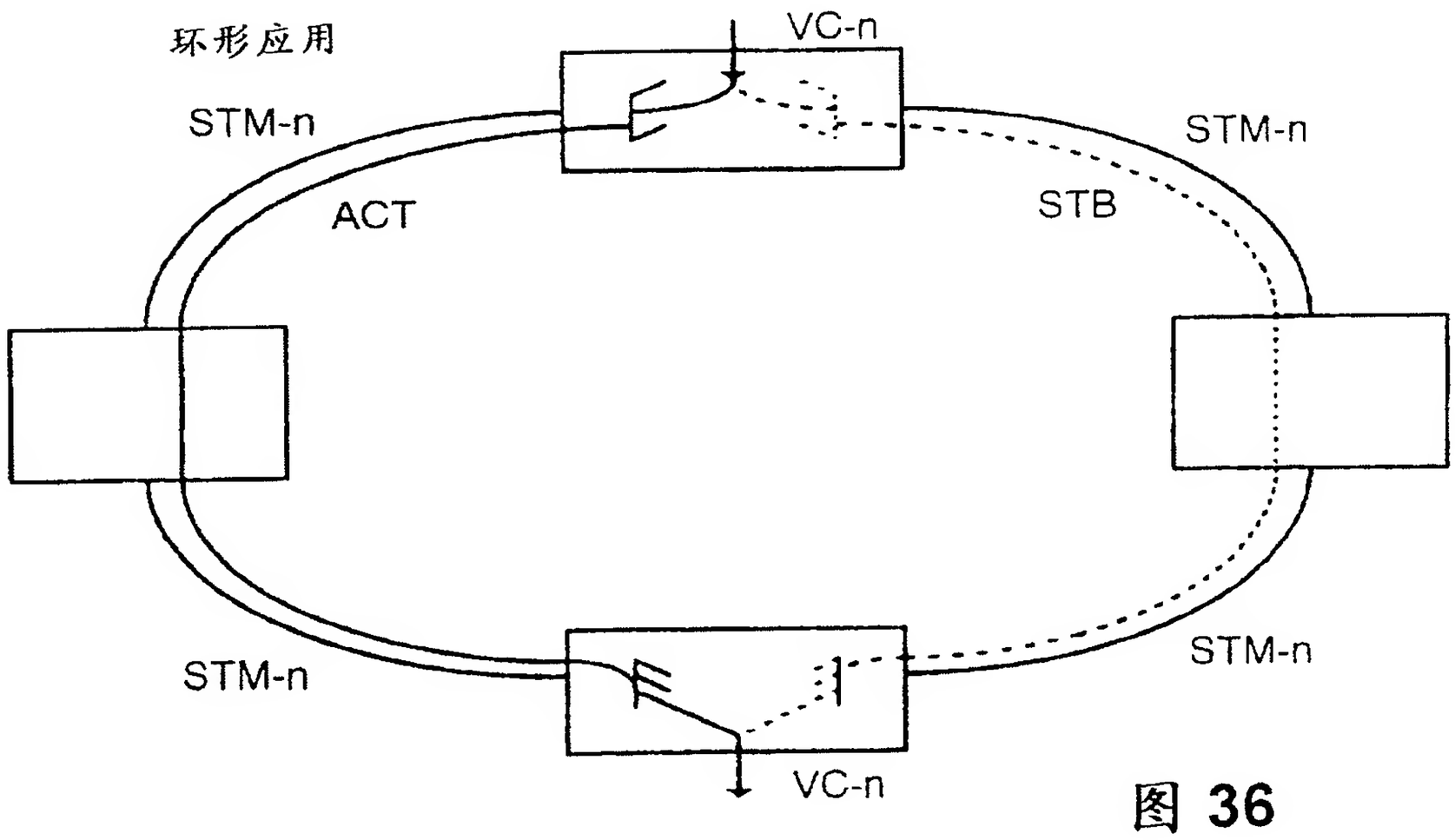

环形应用
VC-n
STM-n
ACT
STB
STM-n
STM-n
STM-n
VC-n

图 36

Integrated cross switch unit and service scheduling method thereof

Publication number: CN1633103 (A)
Publication date: 2005-06-29
Inventor(s): HE JIANFEI [CN] +
Applicant(s): HUAWEI TECH CO LTD [CN] +
Classification:
- international: ***H04J3/00; H04J3/14; H04J 3/16;*** *H04L12/56;* **H04J3/00; H04J3/14; H04J3/16;** H04L12/56; (IPC1-7): H04J3/00; H04L12/56
- European: H04J3/16A2A
Application number: CN20031121799 20031224
Priority number(s): CN20031121799 20031224

Also published as:
CN100428732 (C)
EP1699153 (A1)
EP1699153 (A4)
EP1699153 (B1)
US2007258444 (A1)
more >>

Abstract of **CN 1633103 (A)**
This invention relates an integrated crossing exchange unit and its service dispatch method. The exchange unit includes a bus identifying module, a cross module, an image/de-image module, a package/de-package module and a packet scheduling module. The bus identifying module identifies the service source and delivers the service from SDH circuit unit to the crossed module to realize TDM service cross and sends the data service to a packet scheduling module for scheduling by an image/de-image module, a package/de package module. The data packet from data process unit is sent to the packet schedule module for scheduling.

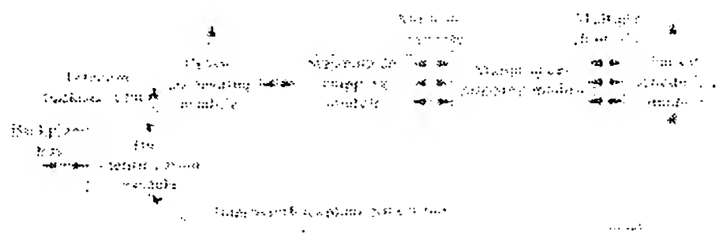


FIG. 2

Integrated cross switch unit and service scheduling method thereof

Description not available for **CN 1633103 (A)**
Description of corresponding document: **EP 1699153 (A1)**

Field of the Invention

[0001] The present invention relates to cross-connecting and switching technology of TDM (Time Division Multiplexing) service and data service in communication systems.

Background of the Invention

[0002] As the data service increases, the conventional SDH (Synchronous Digital Hierarchy) transmission technology also has corresponding advancement. The Next Generation SDH (NG SDH) technology represented by virtual concatenation, LCAS (Link Capacity Adjustment Scheme) and GFP (Generic Framing Procedure) accelerates the evolution of conventional SDH devices mainly-designed for TDM service to the direction of MSTP (Multi-Service Transmission Platform).

[0003] In MSTP devices, switching of data service between different boards can be implemented through adding data switching function, and accordingly, the demand of incremental data service can be satisfied.

[0004] At present, almost all data switching and TDM cross-connecting are implemented on different boards; some solutions can accomplish data/TDM integrated switching, but these solutions have some problems, the most important one of which is they need line boards to implement identification of data service, and even de-mapping and de-encapsulation; in this way, the virtual concatenation service in different lines can not be supported.

[0005] FIG.1 shows a data switching solution of the prior art. In this solution, a data service processing unit transmits the data as required to be switched to a data switching unit via data bus to implement switching; a line unit implements separation of data service and TDM service on SDH lines, so that the data service gets to the data switching unit via the data bus to be switched, and the TDM service is crossed by a cross-connecting unit.

[0006] The data switching unit may has functions of encapsulating and mapping data service to SDH container, here the data switching unit is connected with the cross-connecting unit by the bus.

[0007] It can be seen from the above, the prior art has following disadvantages:
(1) The cross-connecting unit for TDM service and the Switching Unit for data service are separated, low-integration, and occupying relatively more system slots;
(2) The line unit needs to implement separation of data service and TDM service, in the circumstances of virtual concatenation, the same service is possible to born at different line units through different routes, then the line unit can not implement separation of data service and TDM service.

Summary of the Invention

[0008] In view of the disadvantages of the prior art, an embodiment of the present invention aims to provide an integrated cross-switching unit to integrate the functions of TDM cross-connecting and data switching into the same unit, which reduces the demand of system slots; another embodiment of the present invention aims to provide a service scheduling method using the above integrated cross-switching unit.

[0009] The integrated cross-switching unit according to an embodiment of the present invention, used for SDH system comprising an SDH line unit and a data service processing unit, including: a bus identification module, a cross-connecting module, a mapping/de-mapping module, an encapsulation/de-encapsulation module, and a packet scheduling module; wherein
the bus identification module transmits the data service and/or TDM service from the SDH line unit to the cross-connecting unit and transmits the data service from the data service processing unit to the packet scheduling module;
the cross-connecting module implements cross-scheduling for time slots of the TDM service, and schedules the time slots corresponding to the data service from the SDH line unit to the mapping/de-mapping module;
the mapping/de-mapping module receives data frames from the cross-connecting module, and implements mapping for the data from the encapsulation/de-encapsulation module;
the encapsulation/de-encapsulation module receives the data frames from the mapping/de-mapping module, implements data link layer de-encapsulation, and encapsulates the packets from the packet scheduling module;
the packet scheduling module receives the data packets from the encapsulation/de-encapsulation module and/or the bus identification module to implement packet scheduling based on label; transmitting the scheduled data to the data service processing unit via packet bus or to the SDH line unit via the encapsulation/de-encapsulation module, the mapping/de-mapping module and the cross-connecting unit in turn.

[0010] Preferably, multiple physical channels are configured between the mapping/de-mapping module and the encapsulation/de-encapsulation module, and between the encapsulation/de-encapsulation module and the packet scheduling module.

[0011] Preferably, the multiple physical channels are respectively configured with different encapsulation protocols.

[0012] Preferably, for the GFP frames from different physical channels, the encapsulation/de-encapsulation module finds CID field in the extended header of each GFP frame and forwards directly the data frame with the CID field into the corresponding physical channel.

[0013] Another aspect of the present invention aims to provide an integrated cross-switching unit, used for SDH system including an SDH line unit and a data service processing unit, including: a bus identification module, a high-order cross-connecting module, a high-order mapping/de-mapping module, a high-order encapsulation/de-encapsulation module, a high-order packet scheduling module, a low-order cross-connecting module, a low-order mapping/de-mapping module, a low-order encapsulation/de-encapsulation module, and a low-order packet scheduling module; wherein
the bus identification module transmits the data service and/or TDM service from the SDH line unit to the high-order cross-connecting unit, and transmits the data service from the data service processing unit to the high-order packet

scheduling module;
the high-order cross-connecting module schedules the service as required for low-order processing to the low-order cross-connecting module, implements cross-scheduling for time slots of high-order TDM service, and schedules the time slots corresponding to the high-order data service from the SDH line unit to the high-order mapping/de-mapping module;
the low-order cross-connecting module implements cross-scheduling for time slots of low-order TDM service, and schedules the time slots corresponding to low-order data service from the SDH line unit to the low-order mapping/de-mapping module;
the high-order and low-order mapping/de-mapping modules receive the data frames from the high-order and low-order cross-connecting modules correspondingly, and implement mapping for the data from the high-order and low-order encapsulation/de-encapsulation modules respectively;
the high-order and low-order encapsulation/de-encapsulation modules receive the data frames from the high-order and low-order mapping/de-mapping modules correspondingly, implement data link layer de-encapsulation, and encapsulate the packets from the high-order and low-order packet scheduling modules;
the high-order packet scheduling module receives the data packets from the high-order encapsulation/de-encapsulation module and/or the bus identification module and implements packet scheduling based on label; transmitting the scheduled data to the data service processing unit via packet bus or to the SDH line unit via the high-order encapsulation/de-encapsulation module, the high-order mapping/de-mapping unit and the high-order cross-connecting module in turn;
the low-order packet scheduling module receives the data packets from the low-order encapsulation/de-encapsulation module and implements packet scheduling based on label; transmitting the scheduled data to the SDH line unit via the low-order encapsulation/de-encapsulation module, the low-order mapping/de-mapping unit and the low-order cross-connecting module in turn. The low-order packet scheduling module receives the data packets from the low-order encapsulation/de-encapsulation module and implements packet scheduling based on label; the data after scheduling are transmitted to the data service processing unit through Packet Bus or get to the SDH Unit through low-order encapsulation/de-encapsulation module, low-order Mapping/De-mapping Unit and low-order cross-connecting module in turn.

[0014] A further aspect of the present invention aims to provide a service scheduling method implemented by the above integrated cross-switching unit, including the steps of:
A) the bus identification module transmitting the data service and/or TDM service from the SDH line unit to the cross-connecting module, and going to step B); transmitting the data service from the data service processing unit to the packet scheduling module, and going to step C);
B) the cross-connecting module implementing cross-scheduling for time slots of the TDM service, and transmitting the scheduled data to the SDH line unit; or scheduling the time slots corresponding to the data service from the SDH line unit to the mapping/de-mapping module, the encapsulation/de-encapsulation module receiving the data service from the mapping/de-mapping module and transmitting the data service to the packet scheduling module, and going to step C);
C) the packet scheduling module implementing packet scheduling for the data service; transmitting the scheduled data to the data service processing unit via packet bus, or to the SDH line unit via the encapsulation/de-encapsulation module, the mapping/de-mapping module and the cross-connecting module in turn.

[0015] Preferably, the bus identification module reports the slot number corresponding to the data service processing unit and unit type of the data service processing unit to the control unit via the data service processing unit, and identifies the type of the bus connected with the processing unit as backplane packet bus to identify service source.

[0016] Preferably, the SDH line unit and the data service processing unit copy the service to a first integrated cross-switching unit and a second integrated cross-switching unit which have completely same function and structure to implement the same service scheduling procedure; if the first integrated cross-switching unit and the second integrated cross-switching unit are both normal, the SDH line unit and the data service processing unit receive the same service streams from the first integrated cross-switching unit and the second integrated cross-switching unit, and select either of them to implement a processing based on the service streams; if either of the first integrated cross-switching unit and the second integrated cross-switching unit goes wrong, the faulted integrated cross-switching unit reports to the control unit, and the control unit instructs the SDH line unit and the data service processing unit to select the service stream of the normal integrated cross-switching unit.

[0017] Preferably, the SDH line unit and the data service processing unit copy the service to the first integrated cross-switching unit and the second integrated cross-switching unit which have completely same function and structure to implement the same service scheduling procedure; the SDH line unit and the data service processing unit receive the same service streams from the first integrated cross-switching unit and the second integrated cross-switching unit, and determine whether the two service streams are normal, select either of them and implement a processing based on the service streams if the two service streams are both normal; if either of them is abnormal, select the normal service stream.

[0018] Preferably, the SDH line unit and the data service processing unit allocate the service to the first integrated cross-switching unit and the second integrated cross-switching unit which have completely same function and structure to implement service scheduling; if the first integrated cross-switching unit and the second integrated cross-switching unit are both normal, the SDH line unit and the data service processing unit receive the service streams from the first integrated cross-switching unit and the second integrated cross-switching unit to implement a processing based on the service streams; if either of the first integrated cross-switching unit and the second integrated cross-switching unit goes wrong, the faulted integrated cross-switching unit reports to the control unit, and the control unit instructs the SDH line unit and the data service processing unit to switch the service allocated to the faulted integrated cross-switching unit to the normal integrated cross-switching unit.

[0019] Preferably, the SDH line unit and the data service processing unit allocate the service to the first integrated cross-switching unit and the second integrated cross-switching unit which have completely same function and structure to implement service scheduling; the SDH line unit and the data service processing unit receive the service streams from the first integrated cross-switching unit and the second integrated cross-switching unit and determines whether the service streams are normal; if either of the service streams is abnormal, switch the service of the integrated cross-switching unit corresponding to the abnormal service stream to the normal integrated cross-switching unit.

[0020] Preferably, the service allocated to the first integrated cross-switching unit and the second integrated cross-switching unit has priority; when either of the integrated cross-switching units goes wrong and needs service switching, the high-priority service can substitute the low-priority service under processing.

[0021] Compared with the prior art, the advantageous effect of the present invention include: first, an embodiment of the

present invention provides an integrated cross-switching unit in a system, which saves system slots using the integrated cross-switching unit under the precondition of implementing the same data switching. Secondly, since an embodiment of the present invention includes a bus identification module for identifying service source, and a cross-connecting module can implement separation of TDM service and data service, so the line unit and the data service processing unit can be simplified and suppo rt virtual concatenation.

[0022] Embodiments of the present invention can provide service scheduling on GFP level without de-encapsulation, reducing scheduling time and implementation cost.

[0023] Embodiments of the present invention can realize multi-granularity mapping/de-mapping;

[0024] Embodiments of the present invention can support multiple encapsulation protocols and respectively configure each channel with a different encaps ulation protocol.

[0025] Embodiments of the present invention also can reduce complexity of the data service processing unit, when the access quantity of service is relatively large, it can reduce the total cost of the system effectively.

[0026] It is easier for embodiments of the present invention to realize relatively large service scheduling capacity through separation of high-order service and low-order service.

[0027] Embodiments of the present invention can directly connect the packet service from the service processing unit to the packet scheduling unit to implement scheduling through identification of backplane bus.

Brief Description of the Drawings

[0028]
FIG.1 is a schematic diagram illustrating a service scheduling solution in the prior art;
FIG.2 is a block diagram illustrating the structure of an integrated cross-switching unit according to an embodiment of the present invention;
FIG.3 is a schematic diagram illustrating the connection of implementing 1+1 or 1:1 protection of the integrated cross-switching unit according to an embodiment of the present invention;
FIG.4 is a block diagram illustrating the structure of an integrated cross-switching unit according to another embodiment of the present invention;
FIG.5 is a block diagram illustrating the internal structure of the date service processing unit according to an embodiment of the present invention.

Detailed Description of the Embodiments

[0029] FIG.2 is a block diagram illustrating the structure of an integrated cross-switching unit according to an embodiment of the present invention. The integrated cross-switching unit includes: a bus identification module, a cross-connecting module, a mapping/de-mapping module, an encapsulation/de-encapsulation module, and a packet scheduling module; the bus identification module is connected with a conventional SDH line unit and a data service processing unit, for identifying service source and transmitting the service to the corresponding following parts to implement scheduling.

[0030] For conventional TDM service, the cross-connecting module schedules TDM data of one time slot to another time slot through space-division or time-division, implementing cross-scheduling; for data service from the conventional SDH line unit, which is probably mixed with TDM service, the time slots corresponding to the data service are scheduled to the mapping/de-mapping module by the cross-connecting module, pass the mapping/de-mapping module and the encapsulation/de-encapsulation module in turn, and get to the packet scheduling module, implementing final scheduling.

[0031] The service from the data service processing unit enters the integrated cross-switching unit via backplane packet bus. The bus identification module of the integrated cross-switching unit identifies the backplane packet bus according to the type of the single board plugging in the slot corresponding to the main control unit, and extracts the data packets from the bus, and transmits them to the packet scheduling module to implement scheduling. The scheduled data can be transmitted to the data service processing unit via the packet bus, or can get to the backplane TELECOM bus through the mapping/de-mapping module, the encapsulation/de-encapsulation module and the cross-connecting module and then get to the line unit, in order to implement the processing of packet over SDH.

[0032] The mapping/de-mapping module is used to load data frames into a virtual container or a virtual container group, or extracts data frames from a virtual container or a virtual container group. Virtual container group refers to multiple virtual containers bound together through adjacent concatenations or virtual concatenations. In the embodiment of the present invention, the mapping/de-mapping module of the integrated cross-switching unit supports multi-granularity virtual container or virtual container group, so that service scheduling between virtual containers or virtual container groups with different granularity can be implemented, for example, from VC12 to VC3. For SDH, the granularity of virtual container includes but is not limited to VC12, VC3 and VC4. For SONET (synchronous optical network), the granularity of virtual container includes but is not limited to VT1.5, STS-1, STS-3C etc.

[0033] When virtual concatenation is adopted, the mapping/de-mapping module also implements LCAS (Link Capacity Adjustment Scheme) protocol.

[0034] The encapsulation/de-encapsulation module is used to implement data link layer encapsulation/de-encapsulation of data frames. The data link layer encapsulation is performed for frame alignment.

[0035] In the embodiment of the present invention, the encapsulation/de-encapsulation module of the integrated cross-switching unit supports multiple encapsulation protocols including: GFP (Generic Framing Procedure), LAPS (Link Access Procedure-SDH), HDLC (High-level Data Link Control) etc., so that scheduling of service with different encapsulations can be implemented. Different encapsulation protocols can be respectively configured for each channel.

[0036] Besides common encapsulation/de-encapsulation function, for data streams of linear frames adopting GFP, the encapsulation/de-encapsulation module can implement service scheduling based on CID information in the extended header of GFP frame. That is, for GFP frames from different physical channels (an individual virtual container or virtual container group), the encapsulation/de-encapsulation module can find CID field in the extended header of GFP frame, and forwards the data frames with the CID to corresponding physical channel (an individual virtual container or virtual container group) according to network configuration. This scheduling mechanism can save cost of encapsulation/de-

encapsulation and improve speed of processing.

[0037] The packet scheduling module implements packet scheduling based on label. For a data service frames (de-encapsulating the GFP frame) from different channels, the packet scheduling module finds the label information in the data service frames, and forwards the data frames with the labels into the corresponding channels according to network configuration. Here the label information can be configured differently according to different channels and can exist in different positions in the data frames according to different protocols. The label information can be found according to pre-configured or default offset position. Particularly, the label information can be 802.1Q VLAN label, q-in-q stacked VLAN label, or MPLS L2 VPN label.

[0038] Since the position of the integrated cross-switching unit in the network is very important, an embodiment of the present invention aims to provide a 1+1 or 1:1 protection, as shown in FIG.3.

[0039] When 1+1 protection is provided, the line unit and the data service processing unit copy the service to the integrated cross-switching units A and B, so the service received, processed and transmitted by the integrated cross-switching units A and B are completely same. The line unit and the data service processing unit receive service streams from the integrated cross-switching units A and B, and select either of them to perform a processing based on the service streams.

[0040] When one of the integrated cross-switching units A and B goes wrong, supposing the faulted one is A, then the integrated cross-switching unit A reports to the control unit, and the control unit instructs the line unit and the data service processing unit to select the service streams from the integrated cross-switching unit B. In a different system, the line unit or the data service processing unit can determine the signal is normal or wrong at its receiving end by itself and select the normal one. Here the breakdown includes: performance deterioration or alarm of virtual container overhead detected by the mapping/de-mapping module in the integrated cross-switching unit, performance deterioration or alarm in encapsulation detected by the encapsulation/de-encapsulation module, performance deterioration or alarm of data frames detected by the packet scheduling module, and failure of circuit such as unit power supply, clock etc.

[0041] When 1:1 protection is provided, the service received, processed and transmitted by the integrated cross-switching units A and B are different from each other when they work normally, and moreover the service possibly has priority. When one of the integrated cross-switching units A and B goes wrong, supposing the faulted one is A, then the integrated cross-switching unit A reports to the control unit, and the control unit instructs the line unit and the data service processing unit to switch the service as required to be protected transmitted to A to the service scheduling unit B, and the switched service possibly substitutes for part of the service being processed in B. Which service in B can be substituted is pre-configured, and it may be the service with low priority. In a different system, the line unit or the data service processing unit can determine the signal is normal or wrong at its receiving end by itself and select the normal one. Here the breakdown includes: performance deterioration or alarm of virtual container overhead detected by the mapping/de-mapping module in the integrated cross-switching unit, performance deterioration or alarm in encapsulation detected by the encapsulation/de-encapsulation module, performance deterioration or alarm of data frames detected by the packet scheduling module, and failure of circuit such as unit power supply, clock etc.

[0042] Another embodiment of the present invention provides an integrated cross-switching unit, comprising: a bus identification module, a high-order cross-connecting module, a low-order cross-connecting module, a high-order mapping/de-mapping module, a low-order mapping/de-mapping module, a high-order encapsulation/de-encapsulation module, a low-order encapsulation/de-encapsulation module, a high-order packet scheduling module, and a low-order packet scheduling module. The structure of the integrated cross-switching unit is shown as FIG.4. The capacity of cross-switching is expanded through separation of the high-order and low-order cross-switching. The high-order cross-connecting module schedules the service as required for low-order processing to the low-order cross-connecting module, which implements scheduling of low-order service, and scheduling the service as required for packet scheduling to the low-order mapping/de-mapping module. And the service is in turn processed by the encapsulation/de-encapsulation module and/or the packet scheduling module. The high-order cross-connecting module implements scheduling of high-order service, and the particular procedure of scheduling is as the same as the procedure implemented by the structure in FIG.2, which will not be repeated here. For SDH and SONET, high-order service and low-order service have different definitions, and in general, the high-order service includes speeds of VC3 and VC4; while the low-order service includes speeds of VC3, VC12, VT1.5, etc.

[0043] With the provision of the integrated cross-switching unit, the data service processing unit can be made relatively simple, i.e., only adaptation between the service and the backplane packet bus and addition of label information as required for switching should be implemented. While the complicated service scheduling function, encapsulation function and mapping function are implemented by the integrated cross-switching unit. The block diagram of the data service processing unit is shown as FIG.5. In different applications, other complicated functions can be added in the data service processing unit.

[0044] Here the data service processing unit includes but is not limited to Ethernet service processing unit, SAN service processing unit, ATM service processing unit, FR service processing unit, POS service processing unit, etc.

[0045] The above description is preferred embodiments of the present invention, but does not intend to limit the protection scope of the present invention. It is apparent that various modifications and substitution disclosed within the scope of the present invention by those skilled in the art should be within the disclosed scope of the present invention. Therefore, the protection scope of the present invention should be defined by the appended claims.

Integrated cross switch unit and service scheduling method thereof

Claims not available for **CN 1633103 (A)**
Claims of corresponding document: **EP 1699153 (A1)**

1. An integrated cross-switching unit, which is used for SDH system comprising an SDH line unit and a data service processing unit, comprising:
a bus identification module;
a cross-connecting module;
a mapping/de-mapping module;
an encapsulation/de-encapsulation module; and
a packet scheduling module; wherein
the bus identification module transmits the data service and/or TDM service from the SDH line unit to the cross-connecting unit and transmits the data service from the data service processing unit to the packet scheduling module;
the cross-connecting module implements cross-scheduling for time slots of the TDM service, and schedules the time slots corresponding to the data service from the SDH line unit to the mapping/de-mapping module;
the mapping/de-mapping module receives data frames from the cross-connecting module, and implements mapping for the data from the encapsulation/de-encapsulation module;
the encapsulation/de-encapsulation module receives the data frames from the mapping/de-mapping module, implements data link layer de-encapsulation, and encapsulates the packets from the packet scheduling module;
the packet scheduling module receives the data packets from the encapsulation/de-encapsulation module and/or the bus identification module to implement label-based packet scheduling; transmitting the scheduled data to the data service processing unit via packet bus or to the SDH line unit via the encapsulation/de-encapsulation module, the mapping/de-mapping module and the cross-connecting unit in turn.

2. The integrated cross-switching unit according to claim 1, wherein a plurality of physical channels are configured between the mapping/de-mapping module and the encapsulation/de-encapsulation module, and between the encapsulation/de-encapsulation module and the packet scheduling module.

3. The integrated cross-switching unit according to claim 2, wherein the plurality of physical channels are configured with different encapsulation protocols respectively.

4. The integrated cross-switching unit according to claim 2, wherein for the GFP frames from different physical channels, the encapsulation/de-encapsulation module finds CID field in the extended header of each GFP frame and directly forwards the data frame with the CID field into the corresponding physical channel.

5. An integrated cross-switching unit, which is used for SDH system including an SDH line unit and a data service processing unit, comprising:
a bus identification module;
a high-order cross-connecting module;
a high-order mapping/de-mapping module;
a high-order encapsulation/de-encapsulation module;
a high-order packet scheduling module;
a low-order cross-connecting module;
a low-order mapping/de-mapping module;
a low-order encapsulation/de-encapsulation module; and
a low-order packet scheduling module; wherein
the bus identification module transmits the data service and/or TDM service from the SDH line unit to the high-order cross-connecting module, and transmits the data service from the data service processing unit to the high-order packet scheduling module;
the high-order cross-connecting module schedules the service as required for low-order processing to the low-order cross-connecting module, implements cross-scheduling for time slots of high-order TDM service, and schedules the time slots corresponding to the high-order data service from the SDH line unit to the high-order mapping/de-mapping module;
the low-order cross-connecting module implements cross-scheduling for time slots of low-order TDM service, and schedules the time slots corresponding to the low-order data service from the SDH line unit to the low-order mapping/de-mapping module;
the high-order and low-order mapping/de-mapping modules receive the data frames from the high-order and low-order cross-connecting modules correspondingly, and implement mapping for the data from the high-order and low-order encapsulation/de-encapsulation modules respectively;
the high-order and low-order encapsulation/de-encapsulation modules receive the data frames from the high-order and low-order mapping/de-mapping modules correspondingly, implement data link layer de-encapsulation, and encapsulate the packets from the high-order and low-order packet scheduling modules respectively;
the high-order packet scheduling module receives the data packets from the high-order encapsulation/de-encapsulation module and/or the bus identification module and implements label-based packet scheduling; transmits the scheduled data to the data service processing unit via packet bus or to the SDH line unit via the high-order encapsulation/de-encapsulation module, the high-order mapping/de-mapping unit and the high-order cross-connecting module in turn;
the low-order packet scheduling module receives the data packets from the low-order encapsulation/de-encapsulation module and implements label-based packet scheduling; transmits the scheduled data to the SDH line unit via the low-order encapsulation/de-encapsulation module, the low-order mapping/de-mapping unit and the low-order cross-connecting module in turn.

6. A service scheduling method implemented by the integrated cross-switching unit of claim 1, comprising the steps of:
A) a bus identification module transmitting the data service and/or TDM service from the SDH line unit to the cross-connecting module, and going to step B) ; transmitting the data service from the data service processing unit to the packet scheduling module, and going to step C);
B) the cross-connecting module implementing cross-scheduling for time slots of the TDM service, and transmitting the scheduled data to the SDH line unit; or scheduling the time slots corresponding to the data service from the SDH line unit to the mapping/de-mapping module, the encapsulation/de-encapsulation module receiving the data service from the mapping/de-mapping module and transmitting the data service to the packet scheduling module, and going to step C);
C) the packet scheduling module implementing packet scheduling for the data service; transmitting the scheduled data

to the data service processing unit via packet bus, or to the SDH line unit via the encapsulation/de-encapsulation module, the mapping/de-mapping module and the cross-connecting module in turn.

7. The service scheduling method according to claim 6, wherein the bus identification module reports the slot number corresponding to the data service processing unit and unit type of the data service processing unit to the control unit via the data service processing unit, and identifies the type of the bus connected with the processing unit as backplane packet bus to identify service source.

8. The service scheduling method according to claim 6,
wherein the SDH line unit and the data service processing unit copy the service to a first integrated cross-switching unit and a second integrated cross-switching unit which have the same function and structure to implement the same service scheduling procedure; if the first integrated cross-switching unit and the second integrated cross-switching unit are both normal, the SDH line unit and the data service processing unit receive the same service streams from the first integrated cross-switching unit and the second integrated cross-switching unit , and select either of them to implement a processing based on the service streams; if either of the first integrated cross-switching unit and the second integrated cross-switching unit goes wrong, the faulted integrated cross-switching unit reports to the control unit, and the control unit instructs the SDH line unit and the data service processing unit to select the service stream of the normal integrated cross-switching unit.

9. The service scheduling method according to claim 6,
wherein the SDH line unit and the data service processing unit copy the service to the first integrated cross-switching unit and the second integrated cross-switching unit which have the same function and structure to implement the same service scheduling procedure; the SDH line unit and the data service processing unit receive the same service streams from the first integrated cross-switching unit and the second integrated cross-switching unit , determine whether the two service streams are normal, and select either of them and implement a processing based on the service streams if the two service streams are both normal; if either of them is abnormal, select the normal service stream.

10. The service scheduling method according to claim 6, wherein the SDH line unit and the data service processing unit allocate the service to the first integrated cross-switching unit and the second integrated cross-switching unit which have the same function and structure to implement service scheduling; if the first integrated cross-switching unit and the second integrated cross-switching unit are both normal, the SDH line unit and the data service processing unit receive the service streams from the first integrated cross-switching unit and the second integrated cross-switching unit to implement a processing based on the service streams; if either of the first integrated cross-switching unit and the second integrated cross-switching unit goes wrong, the faulted integrated cross-switching unit reports to the control unit, and the control unit instructs the SDH line unit and the data service processing unit to switch the service allocated to the faulted integrated cross-switching unit to the normal integrated cross-switching unit.

11. The service scheduling method according to claim 6, wherein the SDH line unit and the data service processing unit allocate the service to the first integrated cross-switching unit and the second integrated cross-switching unit which have the same function and structure to implement service scheduling; the SDH line unit and the data service processing unit receive the service streams from the first integrated cross-switching unit and the second integrated cross-switching unit and determine whether the service streams are normal; if either of the service streams is abnormal, switch the service of the integrated cross-switching unit corresponding to the abnormal service stream to the normal integrated cross-switching unit.

12. The service scheduling method according to claim 9 or 10, wherein the service allocated to the first integrated cross-switching unit and the second integrated cross-switching unit has priority; when either of the integrated cross-switching units goes wrong and needs service switching, the high-priority service can substitute the low-priority service under processing.

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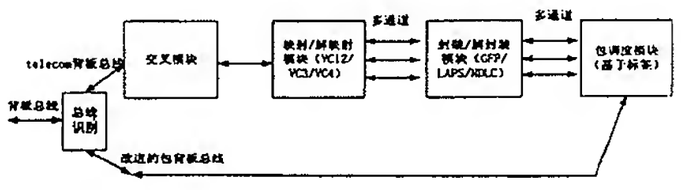
[54] 发明名称

集成交叉交换单元及其业务调度方法

[57] 摘要

本发明有关集成交叉交换单元及其业务调度方法，该集成交叉交换单元包括：一总线识别模块、一交叉模块、一映射/解映射模块、一封装/解封装模块和一包调度模块；由总线识别模块识别出业务来源，将来自 SDH 线路单元的业务送到交叉模块，由交叉模块实现 TDM 业务交叉，并将其中的数据业务通过一映射/解映射模块、一封装/解封装模块送达一包调度模块进行调度；来自数据业务处理单元的数据包则直接送到包调度模块进行调度。 本发明将 TDM 业务和数据业务的交叉、交换功能集成在同一单元中实现，减少了系统槽位要求，并可实现较大容量的业务调度。



1、一种集成交叉交换单元，将TDM业务和数据业务的交叉、交换功能集成在同一单元中实现，其特征在于包括：一总线识别模块、一交叉模块、一映射/解映射模块、一封装/解封装模块和一包调度模块；

所述总线识别模块与SDH线路单元和数据业务处理单元相连接，将来自SDH线路单元的数据业务和/或TDM业务送到交叉模块，将来自数据业务处理单元的数据业务中的数据帧直接送到包调度模块进行包调度；

所述交叉模块实现对TDM业务的时隙交叉调度，并将来自SDH线路单元的数据业务中的数据帧对应的时隙调度到映射/解映射模块；其中，所述时隙交叉调度是指将一个时隙的TDM业务调度到另一个时隙；

所述映射/解映射模块接收来自交叉模块的数据帧，实现数据帧装载到一个虚容器或虚容器组，或从一个虚容器或虚容器组中将数据帧提取出来；

所述封装/解封装模块接收来自映射/解映射模块的数据帧，并进行数据链路层包封，并对来自包调度模块的封包实现解包封，解包封后数据帧被存入一个虚容器或虚容器组；

所述包调度模块接收来自封装/解封装模块和/或总线识别模块的数据帧，实现基于标签的包调度；调度之后的数据，通过包总线送到数据业务处理单元或依次经过封装/解封装模块、映射/解映射模块和交叉模块到达SDH线路单元。

2、如权利要求1所述的集成交叉交换单元，其特征在于：所述封装/解封装模块与所述映射/解映射模块和包调度模块之间设置多个物理通道。

3、如权利要求2所述的集成交叉交换单元，其特征在于：所述多个物理通道分别配置有不同的封装协议。

4、如权利要求2所述的集成交叉交换单元，其特征在于：所述封装/解封装模块对于来自不同物理通道中的GFP帧，找到GFP帧中的扩展头中的CID字段，直接将带有特定CID字段的GFP帧转发到特定的物理通道中。

5、一种集成交叉交换单元，将TDM业务和数据业务的交叉、交换功能集

成在同一单元中实现，其特征在于包括：一总线识别模块、一高阶交叉模块、一高阶映射/解映射模块、一高阶封装/解封装模块、一高阶包调度模块、一低阶交叉模块、一低阶映射/解映射模块、一低阶封装/解封装模块和一低阶包调度模块；

所述总线识别模块与 SDH 线路单元和数据业务处理单元相连接，将来自 SDH 线路单元的数据业务和/或 TDM 业务送到高阶交叉模块，将来自数据业务处理单元的数据业务中的数据帧直接送到高阶包调度模块进行包调度；

所述高阶交叉模块将需要进行低阶处理的业务调度到低阶交叉模块，同时实现对高阶 TDM 业务的时隙交叉调度，并将来自 SDH 线路单元的高阶数据业务中的数据帧对应的时隙调度到高阶映射/解映射模块；其中，所述时隙交叉调度是指将一个时隙的 TDM 数据调度到另一个时隙；

所述低阶交叉模块实现对低阶 TDM 业务的时隙交叉调度，并将来自 SDH 线路单元的低阶数据业务中的数据帧对应的时隙调度到低阶映射/解映射模块；

所述高阶和低阶映射/解映射模块对应接收来自高阶和低阶交叉模块的数据帧，实现数据帧装载到一个虚容器或虚容器组，或从一个虚容器或虚容器组中将数据帧提取出来；

所述高阶和低阶封装/解封装模块对应接收来自高阶和低阶映射/解映射模块的数据帧，并进行数据链路层包封，并分别对来自高阶和低阶包调度模块的封包实现解包封，解包封后数据帧被存入一个虚容器或虚容器组；

所述高阶包调度模块接收来自高阶封装/解封装模块和/或总线识别模块的数据帧，实现基于标签的包调度；调度之后的数据，通过包总线送到数据业务处理单元或依次经过高阶封装/解封装模块、高阶映射/解映射模块和高阶交叉模块到达 SDH 线路单元；

所述低阶包调度模块接收来自低阶封装/解封装模块的数据包，实现基于标签的包调度；调度之后的数据，依次经过低阶封装/解封装模块、低阶映射/解映射模块和低阶交叉模块到达 SDH 线路单元。

6、一种业务调度方法，使用如权利要求 1 所述的集成交叉交换单元，该方法包括下列步骤：

A)总线识别模块将来自 SDH 线路单元的数据业务和/或 TDM 业务送到交叉模块，交叉模块对 TDM 业务进行时隙交叉调度，并将来自 SDH 线路单元的数据业务对应的时隙调度到映射/解映射模块，再经过封装/解封装模块到达包调度模块实现调度；其中，所述时隙交叉调度是指将一个时隙的 TDM 业务调度到另一个时隙；

B）总线识别模块将来自数据业务处理单元的数据业务直接送到包调度模块进行包调度；

C）调度之后的数据，通过包总线送到数据业务处理单元，或依次通过封装/解封装模块、映射/解映射模块和交叉模块到达 SDH 线路单元。

7、如权利要求 6 所述的业务调度方法，其特征在于：使用两个功能、结构完全相同的集成交叉交换单元 A 和 B，SDH 线路单元和数据业务处理单元将业务复制到集成交叉交换单元 A 和 B 进行相同的业务调度过程；若集成交叉交换单元 A 和 B 均正常，则 SDH 线路单元和数据业务处理单元接收来自集成交叉交换单元 A 和 B 相同的业务流，从中选择一份，进行相应处理；若集成交叉交换单元 A 和 B 中有一个发生故障，则由发生故障的集成交叉交换单元上报一控制单元，由控制单元指示 SDH 线路单元和数据业务处理单元选择工作正常的另一集成交叉交换单元的业务流。

8、如权利要求 6 所述的业务调度方法，其特征在于：使用两个功能、结构完全相同的集成交叉交换单元 A 和 B，SDH 线路单元和数据业务处理单元将业务复制到集成交叉交换单元 A 和 B 进行相同的业务调度过程；SDH 线路单元和数据业务处理单元接收来自集成交叉交换单元 A 和 B 相同的业务流并判断两份业务流是否正常，若两份业务流均正常，则从中选择一份，进行相应处理；若有一份业务流异常，则选择正常的业务流。

9、如权利要求 6 所述的业务调度方法，其特征在于：使用两个功能、结

构完全相同的集成交叉交换单元 A 和 B，SDH 线路单元和数据业务处理单元将业务分配给集成交叉交换单元 A 和 B 进行业务调度;若集成交叉交换单元 A 和 B 均正常，则 SDH 线路单元和数据业务处理单元接收来自集成交叉交换单元 A 和 B 的业务流，进行相应处理；若集成交叉交换单元 A 和 B 中有一个发生故障，则由发生故障的集成交叉交换单元上报一控制单元，由控制单元指示 SDH 线路单元和数据业务处理单元将原来分配给发生故障的集成交叉交换单元的业务切换到工作正常的另一集成交叉交换单元。

10、如权利要求 6 所述的业务调度方法，其特征在于：使用两个功能、结构完全相同的集成交叉交换单元 A 和 B，SDH 线路单元和数据业务处理单元将业务分配给集成交叉交换单元 A 和 B 进行业务调度；SDH 线路单元和数据业务处理单元接收来自集成交叉交换单元 A 和 B 的业务流并判断业务流是否正常，若其中一份业务流异常，则将分配给该业务流对应的集成交叉交换单元的业务切换到另一工作正常的集成交叉交换单元。

11、如权利要求 9 或 10 所述的业务调度方法，其特征在于：所述分配给集成交叉交换单元 A 和 B 的业务具有优先级，当一集成交叉交换单元发生故障需要进行业务切换时，高优先级的业务替代正在处理的低优先级的业务。

12、如权利要求 6 所述的业务调度方法，其特征在于所述总线识别模块通过所述数据业务处理单元向控制单元上报所述数据业务处理单元所在槽位和单元类型，将所述数据业务处理单元相连的总线类型识别为包背板总线。

集成交叉交换单元及其业务调度方法

技术领域

本发明涉及通信系统中的 TDM 业务和数据业务的交叉、交换技术，尤指采用一种集成交叉交换单元实现 TDM 业务和数据业务集成调度的方法。

背景技术

随着数据业务的逐渐增多，传统的SDH（Synchronous Digital Hierarchy，同步数字体系）传输技术也发生了相应的进步。以虚级联、LCAS（Link Capacity Adjustment Scheme，链路容量调整机制）、GFP（Generic Framing Procedure，通用成帧规程）为代表的下一代SDH（NG SDH）技术，促进了以TDM（Time division multiplexing，时分复用）业务为主的传统SDH设备向多业务传送平台（MSTP）演进。

在MSTP设备中，通过增加数据交换功能，可以实现不同单板之间数据业务的交换，从而满足数据业务的比例逐步增加的需求。

目前数据交换与TDM交叉基本上是分开在不同单板上实现的；有一些方案完成数据/TDM集成交换，但存在问题：其中最重要的问题是需要在线路单板完成数据业务的识别、甚至解映射、解封装；这样的话，对于走不同线路的虚级联业务，无法支持。

如图 1 所示，为现有技术中的一种数据交换方案，在这种方案中，数据业务处理单元将需要进行交换的数据通过数据总线到达数据交换单元交换；线路单元实现数据业务与 TDM 业务的分离，将数据业务通过数据总线到达数据交换单元交换，将 TDM 业务通过交叉单元交叉。

数据交换单元可能还具备数据业务到 SDH 容器的封装和映射，此时数据交换单元与交叉单元有总线相连。

现有技术的缺点有：

（1）数据交换单元需要冗于保护，占用系统槽位较多；

（2）线路单元需要实现数据业务与TDM业务的分离，对于虚级联的情况，相同的业务可能走不同的路由，出现在不同的线路单元，此时线路单元无法实现数据业务与TDM业务的分离。

发明内容

鉴于现有技术中的缺点，本发明提供一种集成交叉交换单元，实现将 TDM 交叉、数据交换功能集成在同一单元中，减少系统槽位需求，并可以实现较大容量交换能力。

本发明提供一种集成交叉交换单元，实现将 TDM 业务和数据业务的交叉、交换功能集成在同一单元中，包括：一总线识别模块、一交叉模块、一映射/解映射模块、一封装/解封装模块和一包调度模块；

所述总线识别模块与 SDH 线路单元和数据业务处理单元相连接，将来自 SDH 线路单元的数据业务和/或 TDM 业务送到交叉模块，将来自数据业务处理单元的数据业务中的数据帧直接送到包调度模块进行包调度；

所述交叉模块实现对 TDM 业务的时隙交叉调度，并将来自 SDH 线路单元的数据业务中的数据帧对应的时隙调度到映射/解映射模块；其中，所述时隙交叉调度是指将一个时隙的 TDM 业务调度到另一个时隙；

所述映射/解映射模块接收来自交叉模块的数据帧，实现数据帧装载到一个虚容器或虚容器组，或从一个虚容器或虚容器组中将数据帧提取出来；

所述封装/解封装模块接收来自映射/解映射模块的数据帧，并进行数据链路层包封，并对来自包调度模块的封包实现解包封，解包封后数据帧被存入一个虚容器或虚容器组；

所述包调度模块接收来自封装/解封装模块和/或总线识别模块的数据帧，实现基于标签的包调度；调度之后的数据，通过包总线送到数据业务处理单元

或依次经过封装/解封装模块、映射/解映射模块和交叉模块到达SDH线路单元。

根据本发明的上述集成交叉交换单元，所述封装/解封装模块与所述映射/解映射模块和包调度模块之间设置多个物理通道。

根据本发明的上述集成交叉交换单元，所述多个物理通道分别配置有不同的封装协议。

根据本发明的上述集成交叉交换单元，所述封装/解封装模块对于来自不同物理通道中的 GFP 帧，找到 GFP 帧中的扩展头中的 CID 字段，直接将带有特定 CID 字段的 GFP 帧转发到特定的物理通道中。

本发明另提供一种集成交叉交换单元，包括：一总线识别模块、一高阶交叉模块、一高阶映射/解映射模块、一高阶封装/解封装模块、一高阶包调度模块、一低阶交叉模块、一低阶映射/解映射模块、一低阶封装/解封装模块和一低阶包调度模块；

所述总线识别模块与 SDH 线路单元和数据业务处理单元相连接，将来自 SDH 线路单元的数据业务和/或 TDM 业务送到高阶交叉模块，将来自数据业务处理单元的数据业务中的数据帧直接送到高阶包调度模块进行包调度；

所述高阶交叉模块将需要进行低阶处理的业务调度到低阶交叉模块，同时实现对高阶 TDM 业务的时隙交叉调度，并将来自 SDH 线路单元的高阶数据业务中的数据帧对应的时隙调度到高阶映射/解映射模块；其中，所述时隙交叉调度是指将一个时隙的 TDM 业务调度到另一个时隙；

所述低阶交叉模块实现对低阶 TDM 业务的时隙交叉调度，并将来自 SDH 线路单元的低阶数据业务中的数据帧对应的时隙调度到低阶映射/解映射模块；

所述高阶和低阶映射/解映射模块对应接收来自高阶和低阶交叉模块的数据帧，实现数据帧装载到一个虚容器或虚容器组，或从一个虚容器或虚容器组中将数据帧提取出来；

所述高阶和低阶封装/解封装模块对应接收来自高阶和低阶映射/解映射模块的数据帧，并进行数据链路层包封，并分别对来自高阶和低阶包调度模块的

封包实现解包封，解包封后数据帧被存入一个虚容器或虚容器组；

所述高阶包调度模块接收来自高阶封装/解封装模块和/或总线识别模块的数据帧，实现基于标签的包调度；调度之后的数据，通过包总线送到数据业务处理单元或依次经过高阶封装/解封装模块、高阶映射/解映射模块和高阶交叉模块到达 SDH 线路单元；

所述低阶包调度模块接收来自低阶封装/解封装模块的数据包，实现基于标签的包调度；调度之后的数据，依次经过低阶封装/解封装模块、低阶映射/解映射模块和低阶交叉模块到达 SDH 线路单元。

本发明提供一种业务调度方法，使用所述的集成交叉交换单元，该方法包括下列步骤：

A）总线识别模块将来自 SDH 线路单元的数据业务和/或 TDM 业务送到交叉模块，交叉模块对 TDM 业务进行时隙交叉调度，并将来自 SDH 线路单元的数据业务对应的时隙调度到映射/解映射模块，再经过封装/解封装模块到达包调度模块实现调度；其中，所述时隙交叉调度是指将一个时隙的 TDM 业务调度到另一个时隙；

B）总线识别模块将来自数据业务处理单元的数据业务直接送到包调度模块进行包调度；

C）调度之后的数据，通过包总线送到数据业务处理单元，或依次通过封装/解封装模块、映射/解映射模块和交叉模块到达 SDH 线路单元。

根据本发明的上述方法，使用两个功能、结构完全相同的上述集成交叉交换单元 A 和 B，SDH 线路单元和数据业务处理单元将业务复制到集成交叉交换单元 A 和 B 进行相同的业务调度过程；若集成交叉交换单元 A 和 B 均正常，则 SDH 线路单元和数据业务处理单元接收来自集成交叉交换单元 A 和 B 相同的业务流，从中选择一份，进行相应处理；若集成交叉交换单元 A 和 B 中有一个发生故障，则由发生故障的集成交叉交换单元上报一控制单元，由控制单元指示 SDH 线路单元和数据业务处理单元选择工作正常的另一集成交叉交换单元的业务流。

根据本发明的上述方法，使用两个功能、结构完全相同的上述集成交叉交

换单元 A 和 B，SDH 线路单元和数据业务处理单元将业务复制到集成交叉交换单元 A 和 B 进行相同的业务调度过程；SDH 线路单元和数据业务处理单元接收来自集成交叉交换单元 A 和 B 相同的业务流并判断两份业务流是否正常，若两份业务流均正常，则从中选择一份，进行相应处理；若有一份业务流异常，则选择正常的业务流。

根据本发明的上述方法，使用两个功能、结构完全相同的上述集成交叉交换单元 A 和 B，SDH 线路单元和数据业务处理单元将业务分配给集成交叉交换单元 A 和 B 进行业务调度；若集成交叉交换单元 A 和 B 均正常，则 SDH 线路单元和数据业务处理单元接收来自集成交叉交换单元 A 和 B 的业务流，进行相应处理；若集成交叉交换单元 A 和 B 中有一个发生故障，则由发生故障的集成交叉交换单元上报一控制单元，由控制单元指示 SDH 线路单元和数据业务处理单元将原来分配给发生故障的集成交叉交换单元的业务切换到工作正常的另一集成交叉交换单元。

根据本发明的上述方法，使用两个功能、结构完全相同的上述集成交叉交换单元 A 和 B，SDH 线路单元和数据业务处理单元将业务分配给集成交叉交换单元 A 和 B 进行业务调度；SDH 线路单元和数据业务处理单元接收来自集成交叉交换单元 A 和 B 的业务流并判断业务流是否正常，若其中一份业务流异常，则将分配给该业务流对应的集成交叉交换单元的业务切换到另一工作正常的集成交叉交换单元。

根据本发明的上述方法，所述分配给集成交叉交换单元 A 和 B 的业务具有优先级，当一集成交叉交换单元发生故障需要进行业务切换时，高优先级的业务替代正在处理的低优先级的业务。

所述总线识别模块通过所述数据业务处理单元向控制单元上报所述数据业务处理单元所在槽位和单元类型，将所述数据业务处理单元相连的总线类型识别为包背板总线。

本发明在系统中提供了集成交叉交换单元以及相关的系统结构，可以对

集成交叉交换单元实现 1+1 或 1：1 保护；

本发明可以提供 GFP 层面上的业务调度，不必要解封装，减少调度时间和实现成本。

本发明实现多粒度的映射/解映射；

本发明实现多种封装协议，可对各通道分别配置不同的封装协议。

本发明还可以降低数据业务处理单元的复杂度，当业务接入数量较多的情况下，有效降低系统总的成本。

通过高低阶分离，本发明也相对容易将业务调度容量做得比较大。

通过背板总线的识别，将包业务处理单元过来的包业务直接连接到包调度单元进行调度。

附图说明

图 1 为现有技术中的业务调度方案示意图。

图 2 为本发明的一种集成交叉交换单元结构方框图。

图 3 为本发明实现集成交叉交换单元 1+1 或 1：1 保持的连接示意图。

图 4 为本发明另一集成交叉交换单元结构方框图。

图 5 为本发明的数据业务处理单元内部结构方框图。

具体实施方式

参见图 2，为本发明的一种集成交叉交换单元结构方框图，包括有：总线识别模块、交叉模块、映射/解映射模块、封装/解封装模块和包调度模块；所述总线识别模块与传统 SDH 线路单元和数据业务处理单元相连接，对于传统的 TDM 业务，由交叉模块将一个时隙的 TDM 数据通过空分或时分的方法，调度到另一个时隙，实现交叉调度；对于数据业务，如果来自传统的 SDH 线路单元，可能是与 TDM 业务混合在一起，则通过交叉模块调度，将数据业务对应的时隙调度到映射/解映射模块，然后先后经过映射/解映射模块、

封装/解封装模块，到达包调度模块实现最终的调度。

对于来自数据业务处理单元的业务，通过背板包总线方式进入集成交叉交换单元，集成交叉交换单元的总线识别模块根据主控单元对槽位上所插单板的类型识别出是背板包总线，将数据包从总线中提取出来，传递到包调度模块实现调度。调度之后的数据，可以通过包总线送到数据业务处理单元，也可以经过封装/解封装模块、映射/解映射模块、交叉模块，然后到背板的TELECOM 总线，到达线路单元，实现包 over SDH（SDH 对包的承载）的处理。

映射/解映射模块主要实现数据帧装载到一个虚容器或虚容器组，或从一个虚容器或虚容器组中将数据帧提取出来。虚容器组是指，通过相邻级联或虚级联实现捆绑在一起的数个虚容器。本发明中的集成交叉交换单元的映射/解映射模块支持多种粒度虚容器或虚容器组，以便实现不同粒度虚容器或虚容器组业务之间的调度，比如 VC12 到 VC3。虚容器粒度对 SDH 有但不仅有 VC12、VC3、VC4，对 SONET（synchronous optical network ，同步光网络）有但不仅有，VT1.5、STS-1、STS-3C 等。

但采用虚级联时，映射/解映射模块还实现 LCAS（Link Capacity Adjustment Scheme， 链路容量调整机制）协议。

封装/解封装模块主要实现数据帧的数据链路层包封和解包封。数据链路层包封的主要目的是为了定帧。

本发明中的集成交叉交换单元的封装/解封装模块支持多种封装协议，主要有 GFP（Generic Framing Procedure，通用成帧规程）、LAPS（Link Access Procedure-SDH， 链路接入协议-SDH）、HDLC（High_level Data Link Control， 高级数据链路控制规程）等，以便实现不同封装业务之间的调度。可对各通道分别配置不同的封装协议。

除了一般的封装/解封装功能，对于采用 GFP 的线性帧的数据流，封装/解封装模块可以实现基于 GFP 扩展帧头中的 CID 信息的业务调度。即对于

来自不同物理通道（一个单独的虚容器或虚容器组）中的 GFP 帧，封装/解封装模块可以找到 GFP 帧中的扩展头中的 CID 字段，根据网络的配置，将带有特定 CID 的数据帧转发到特定的物理通道中（一个单独的虚容器或虚容器组）。这种调度机制可以节省封装/解封装的代价，提高处理的速度。

包调度模块主要是基于标签的包调度。即对于来自不同通道中的数据业务帧（去掉了 GFP 封装），包调度模块找到数据业务帧中的标签信息，根据网络的配置，将带有特定标签的数据帧转发到特定的通道中。这里的标签信息根据不同的通道可以有不同的设置，根据不同的协议，在数据帧中可能存在不同的位置。可以通过预配置或缺省的偏移位置找到标签信息。具体地，标签信息可能是 802.1Q 的 VLAN 标签，q-in-q 的 stacked VLAN 标签，MPLS L2 VPN 的标签（label）。

由于集成交叉交换单元在网络中的位置是非常重要的，本发明提供一种 1+1 或 1：1 保护的方法如图 3 所示。

当提供 1+1 保护的时候，线路单元、数据业务处理单元将业务复制到集成交叉交换单元 A 与 B，所以集成交叉交换单元 A、B 接收、处理、发送的业务是完全相同的。线路单元、数据业务处理单元接收到来自集成交叉交换单元 A 与 B 相同的业务流，从中选择一份，进行相应处理。

当集成交叉交换单元 A 与 B 中有一个发生故障，假设为 A，A 上报控制单元，控制单元指示线路单元或数据业务处理单元选择来自 B 的业务流。在不同的系统中，线路单元或数据业务处理单元可以自己从接收端判别信号是正常的，还是故障，并进行选择。这里的故障包括集成交叉交换单元中的映射/解映射模块检测到的虚容器开销的性能劣化、告警，包括封装/解封装模块检测到的封装中的性能劣化、告警，包括包调度模块检测到的数据帧的性能劣化、告警，也包括如单元供电电源、时钟等电路的失效等等。

当提供 1：1 保护的时候，当正常工作的时候，集成交叉交换单元 A、B 接收处理、发送的业务是不相同的，而且业务之间可能是有优先级的。当集

成交叉交换单元 A 与 B 中有一个发生故障，假设为 A，A 上报控制单元，控制单元指示线路单元或数据业务处理单元单元将原来给 A 的业务中，需要保护的部分，切换到业务调度单元 B，切换后可能替代了原来 B 正在处理的业务。B 中哪些业务被替代是预先设置好的，可能是低优先级的业务。在不同的系统中，线路单元或数据业务处理单元可以自己从接收端判别信号是正常的，还是故障，并进行选择。这里的故障包括集成交叉交换单元中的映射/解映射模块检测到的虚容器开销的性能劣化、告警，包括封装/解封装模块检测到的封装中的性能劣化、告警，包括包调度模块检测到的数据帧的性能劣化、告警，也包括如单元供电电源、时钟等电路的失效等等。

本发明另提供一种集成交叉交换单元，其结构如图 4 所示，包括有总线识别模块、高阶和低阶交叉模块、高阶和低阶映射/解映射模块、高阶和低阶封装/解封装模块和高阶和低阶包调度模块；通过高、低阶交叉交换分离来扩展交叉交换的容量。高阶交叉模块将需要进行低阶处理的业务调度到低阶交叉模块，低阶交叉模块实现低阶业务的调度，将需要进行包调度的业务调度到低阶映射/解映射模块，再通过封装/解封装模块和/或包调度模块的处理。高阶交叉模块实现高阶业务的调度，其具体的调度实现过程与图 2 所示结构的调度过程相同，不再重述。高阶、低阶业务对 SDH 和 SONET 体系定义不同，一般高阶包括 VC3、VC4；低阶包括 VC3、VC12、VT1.5 等速率。

提供集成交叉交换单元之后，数据业务处理处理单元可以做得比较简单，只需要实现业务到背板包总线的适配，以及添加交换所需的标签信息。而复杂的业务调度功能、封装和映射功能放在集成交叉交换单元实现。数据业务处理单元的框图如图 5 所示。根据不同的应用，数据业务处理单元也可以增加一些其他复杂的功能。

这里的数据业务处理单元包括但不限于以太网业务处理单元、SAN 业务处理单元、ATM 业务处理单元、FR 业务处理单元、POS 业务处理单元等等。

以上所述，仅为本发明较佳的具体实施方式，但本发明的保护范围并不

局限于此，任何熟悉本技术领域的技术人员在本发明揭露的技术范围内，可轻易想到的变化或替换，都应涵盖在本发明的保护范围之内。因此，本发明的保护范围应该以权利要求书的保护范围为准。

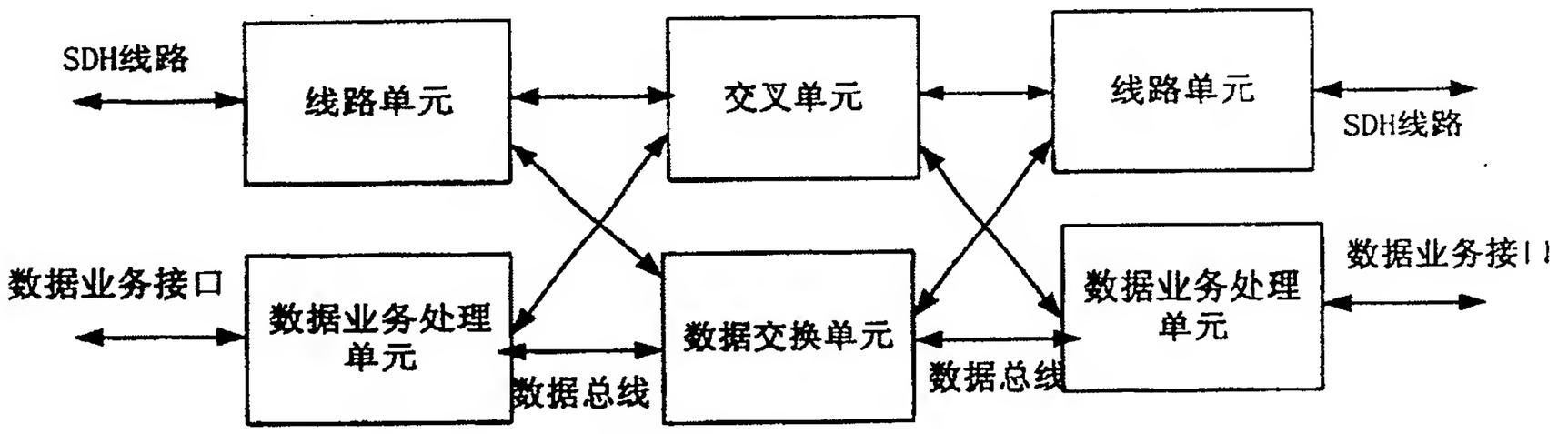

SDH线路
线路单元
交叉单元
线路单元
SDH线路
数据业务接口
数据业务处理单元
数据交换单元
数据业务处理单元
数据业务接口
数据总线
数据总线

图 1

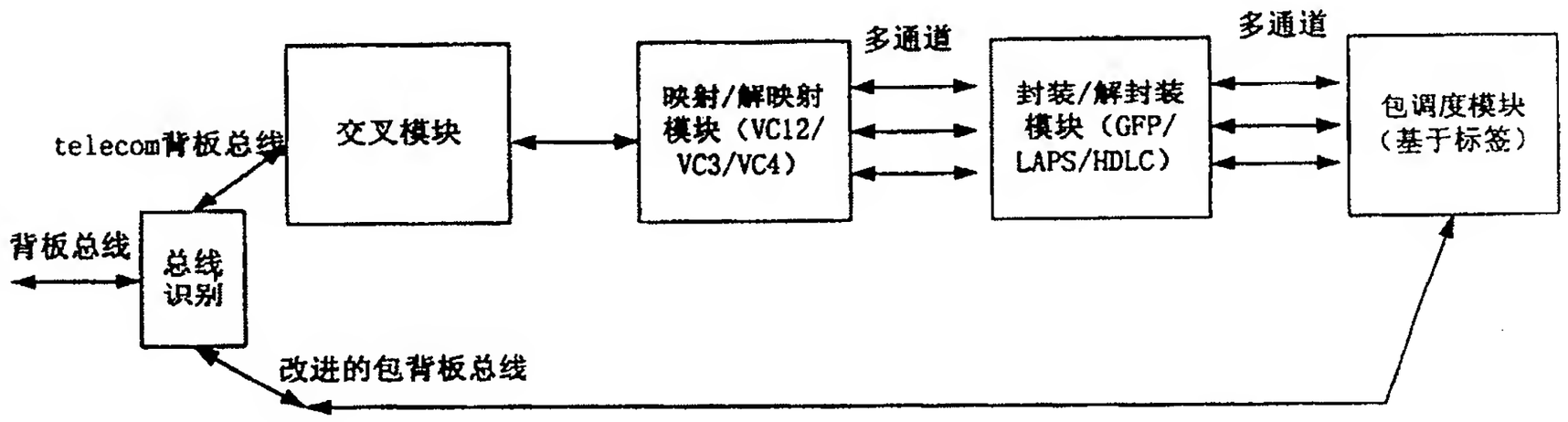

telecom背板总线
交叉模块
映射/解映射模块（VC12/VC3/VC4）
多通道
封装/解封装模块（GFP/LAPS/HDLC）
多通道
包调度模块（基于标签）
背板总线
总线识别
改进的包背板总线

图 2

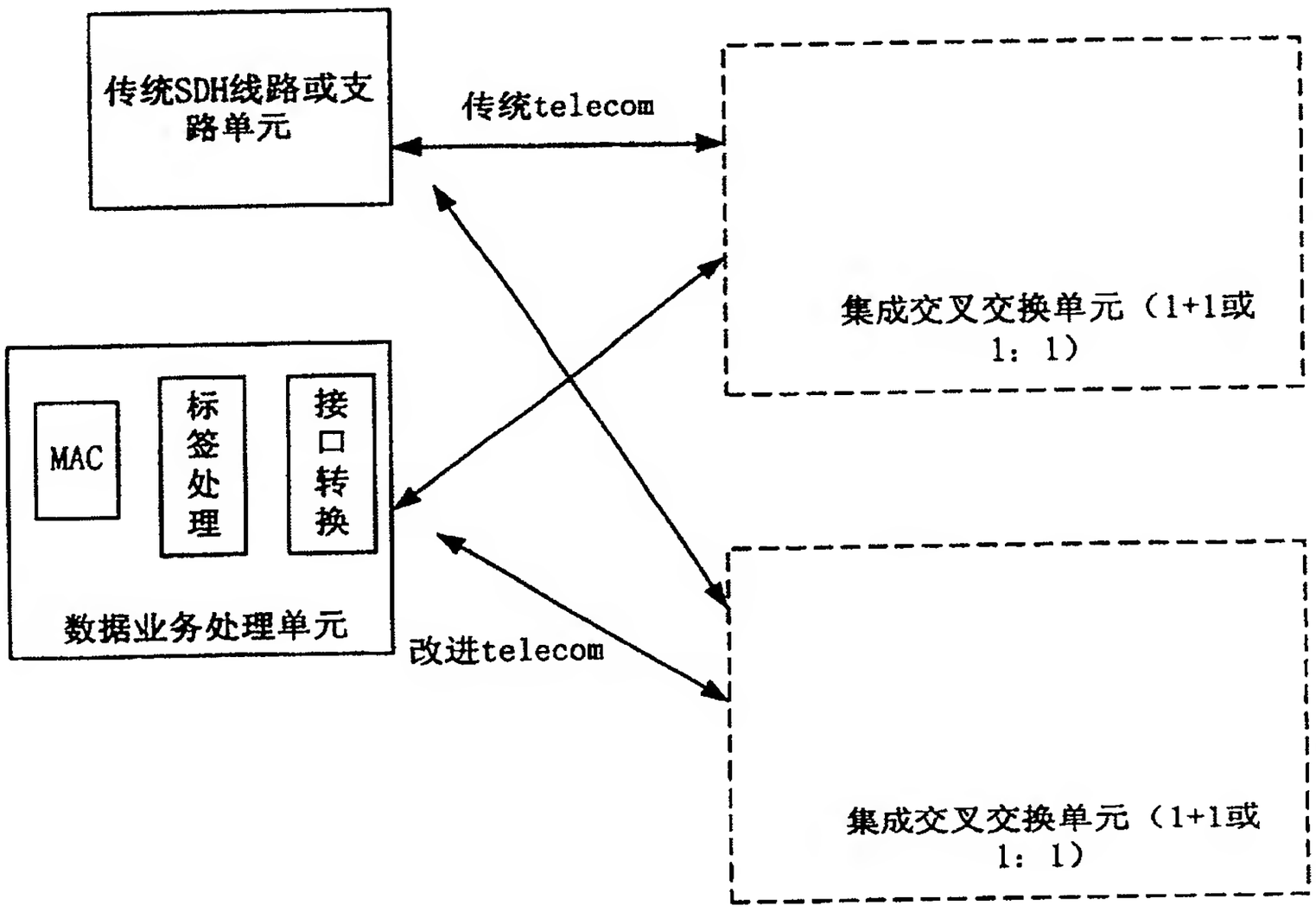

传统SDH线路或支路单元
传统telecom
集成交叉交换单元（1+1或1：1）
MAC
标签处理
接口转换
数据业务处理单元
改进telecom
集成交叉交换单元（1+1或1：1）

图 3

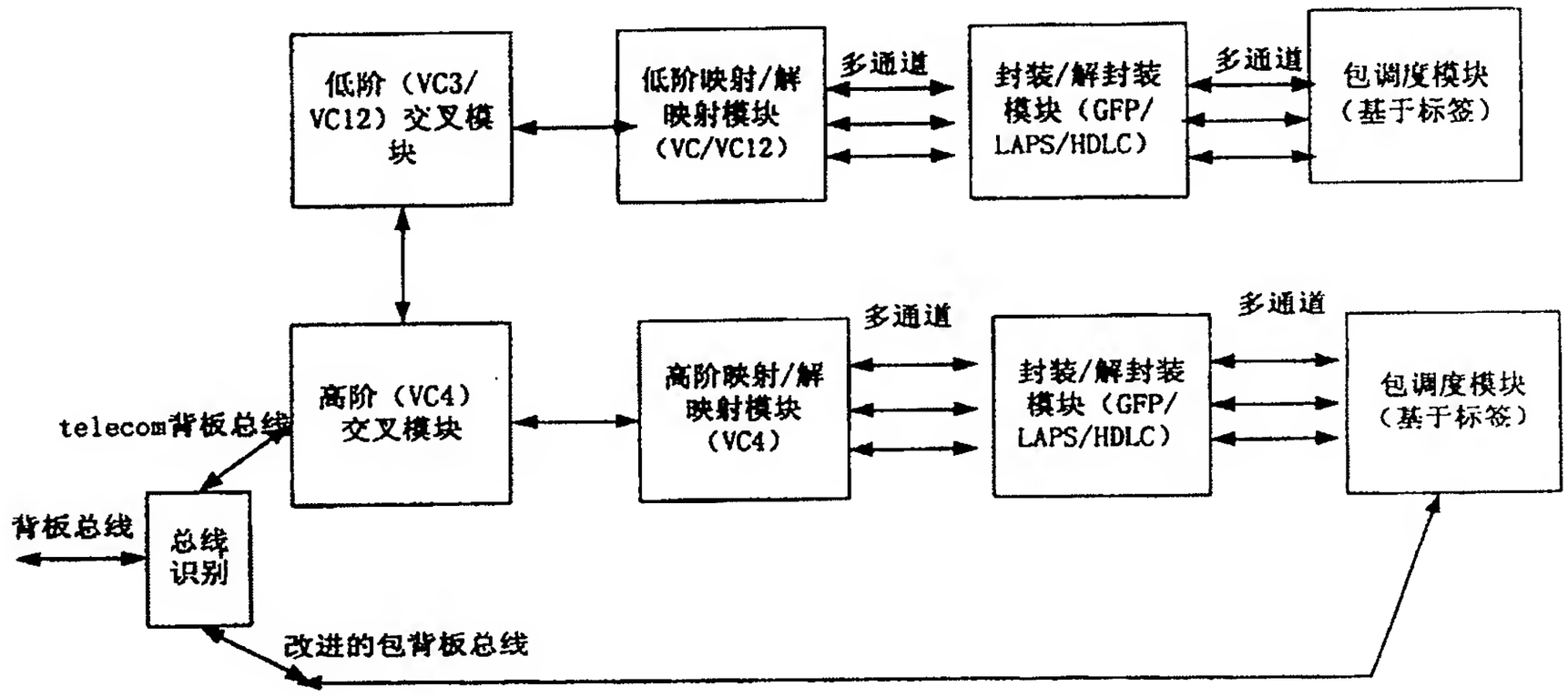

低阶（VC3/VC12）交叉模块
低阶映射/解映射模块（VC/VC12）
多通道
封装/解封装模块（GFP/LAPS/HDLC）
多通道
包调度模块（基于标签）
高阶（VC4）交叉模块
telecom背板总线
高阶映射/解映射模块（VC4）
多通道
封装/解封装模块（GFP/LAPS/HDLC）
多通道
包调度模块（基于标签）
背板总线
总线识别
改进的包背板总线

图 4

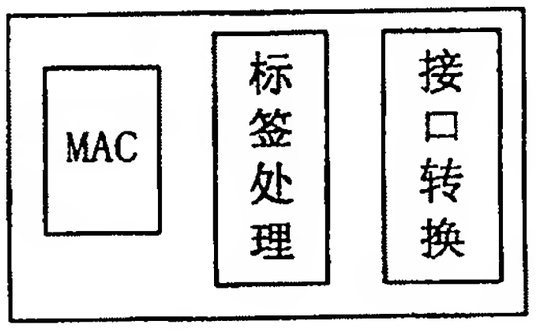

MAC
标签处理
接口转换

图 5